WELDING OF SEMICONDUCTOR NANOWIRES: INITIAL JOINING METHODS, OHMIC JUNCTION FORMATION AND SCALE UP

Thomas Anthony Celano

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Approved by:

James Cahoon

Yosuke Kanai

Wei You

Scott Warren

Andrew Moran

ABSTRACT

Thomas Anthony Celano: Ohmic Welding of Semiconductor Nanowire Networks
(under the direction of James Cahoon)

Single nanowires (NW) have been utilized in a variety of technological applications including optics, energy harvesting, biological/mechanical sensing, electrode scaffolds and other electronic devices. Metallic NW networks have even begun to replace traditional transparent conducting oxides (TCO) in touchscreen electronics, due to the simple solution phase growth and welding processes required to form the network. Unfortunately, semiconductor nanowires exhibit unique challenges during scale-up. One large benefit to semiconductor NWs when compared to metallic analogs, is semiconductor NWs can have functionality encoded via dopant incorporation in-situ and post growth. Unfortunately, large-scale processing of bottom-up grown semiconductor NWs is difficult - often a multi-stage, time consuming process. To overcome this impediment we have developed a process that welds NWs at each point of contact, generating a dense interconnected network of NWs separated by ohmic and highly crystalline junctions.

Using the Vapor Liquid Solid (VLS) growth process, we collapsed and annealed NWs at temperatures 400 to 600 °C below the bulk melting point of Si and Ge, resulting in a large area interconnected network with variable density, NW diameter and optical response. Junctions are polycrystalline, devoid of native oxide and exhibit low junction resistance. Capillarity induced surface diffusion was used to simulate the welding process across different geometries. We determined that junctions exhibited low resistance and networks exhibited relatively uniform electrical connectivity across large regions. Films were able to be fully removed from growth

substrates and contained within PDMS stamps. The resulting PDMS embedded NW networks were mechanically robust and showed only a minor increase in resistance when compared with an analogous network on a growth substrate. Welded semiconductor NW networks show promise for a variety of technological applications and we believe the weld process can be generalized for different nanomaterials.

ACKNOWLEDGEMENTS

I would like to first thank my wife Kristin for her continued support throughout my time in both undergraduate and graduate school. She pushed me to be the best version of myself, bolstering my spirits when I failed and celebrating with me when I succeeded. My parents deserve credit as catalysts for creativity and interest in science they always taught me to search for the truth both in the world and in oneself.

I would also like to thank my Principle Investigator James Cahoon, his consistent motivation was a source of support. Between many useful talks about science and graduate school, I consider myself immensely privileged to have been part of the Cahoon group since its inception.

I would lastly like to thank my friends and colleagues for the making research a bit more enjoyable and life a bit more exciting. I'll remember the friendships made here and I certainly wish everyone success in the future.

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LIST OF ABBREVIATIONS

AAO	Anodized Aluminum Oxide
AgS	Silver Sulfide
AgS	Silver Sulfide
Ar	Argon
AsH_3	Arsine
a-Si	Amorphous Silicon
Au	Gold
AVC	Active Voltage Contrast
B_2H_6	Diborane
BHF	Buffered Hydrofluoric Acid
Cu	Copper
CVD	Chemical Vapor Deposition
DISS	Diameter Indexed Safety System
DRIE	Deep Reactive Ion Etching
EBL	Electron Beam Lithography
FET	Field Effect Transistor
FFT	Fast Fourier Transform
GaAs	Gallium Arsenide
Ge	Germanium
GeH_4	Germane
H_2	Hydrogen
InAs	Indium Arsenide

IPA	Isopropyl Alcohol
ITO	Indium Tin Oxide
LB	Langmuir Blodgett
LED	Light Emitting Diode
MFC	Mass Flow Controller
MIBK	Methyl Isobutyl Ketone
MMA	Methyl methacrylate
NP	Nanoparticle
NT	Nanotube
NW	Nanowire
PCB	Patterned Circuit Board
Pd	Palladium
PECVD	Plasma Enhanced Chemical Vapor Deposition
PML	Perfectly Matched Layers
PMMA	Polymethyl methacrylate
PVP	Polyvinylpyrrolidone
RJ	Junction Resistance
Si	Silicon
SiC	Silicon Carbide
SiH_4	Silane
SOI	Silicon on Insulator
SS	Stainless Steel
STEM	Scanning Transmission Electron Microscopy

STM	Scanning Tunneling Microscopy
TCO	Transparent Conducting Oxide
TE	Transverse Electric
TEM	Transmission Electron Microscopy
TFT	Thin Film Transistor
Ti	Titanium
TM	Transverse Magnetic
VC	Voltage Contrast
VLS	Vapor Liquid Solid
VO2	Vanadium Oxide
VS	Vapor Solid
VSS	Vapor Solid Solid
W	Tungsten
ZnO	Zinc Oxide
ZnS	Zinc Sulfide

CHAPTER 1: INTRODUCTION

1.1 Semiconductor Nanowire Technological Applications

Bottom-up synthesized semiconductor nanowires (NWs), since discovery, have mainly been demonstrated as "single nanowire devices" for proof-of-concept devices. However, these singe NW devices have been used for a various technologies spanning a vast interdisciplinary spectrum, indicating that reliable ordering and scale up methods must be further developed. For example, Si is useful as a battery anode material in lithium ion batteries due to an extremely high theoretical charge capacity compared to the standard graphite electrode (4200 mAh/g and 372 mAh/g for Si and graphite respectively)[1, 2] but also exhibits delamination from the substrate and material degradation due to volume fluctuations that occur during lithiation. Si NWs have been used to overcome this impediment to some extent, since the 2D confinement of the wire geometry allows for the expansion and contraction without damage to the overall electrode[3]. Additionally, semiconductor NWs are often used as electrodes, due to the high surface area to volume ratio. Photoelectrochemical cells with Si NW[4] electrodes have a high surface to volume ratio, which decreases the time required for carrier collection, but also have significant surface trap states. The small dimensions and variable doping of semiconductor NWs have been used to create transistor devices[5-7], solar cell absorbers[8-10], and a variety of different sensors[7, 11, 12]. Semiconductor NWs of VO_2[13], AgS[14], and ZnO[15] have all been used to create resistive switching memory devices, commonly known as memristors. Resistive switching is often achieved by forming/unforming conductive regions within the wire, which normally consist of higher metallic/conducting species concentration. This is much simpler on the nanoscale as localized

joule heating occurs on a much smaller scale and species can migrate from the surface to form conducting channels within the NW quicker at lower applied voltage. For example, insulting ZnO NWs have been used for memristors due, however, when placed between a Cu contact and Pd contact conducting Cu channels form across the NW surface at low applied bias[16]. The NW geometry confines the Cu ions to avoid spreading along surface defects perpendicular to the current and decreasing the switch time, which can occur when using ZnO thin film instead. While these single wire devices demonstrate the usefulness of NWs as a platform for encoding resistive memory bits, architectures that consist of multiple stacked/crossed memory elements are necessary to create future commercially viable resistive memory devices[17].

Since the diameter of NWs is commonly smaller than visible light (<380 nm), NWs exhibit many interesting optical phenomena. Unlike metallic NWs, which generate surface plasmons and heat during absorption[18], semiconductor NWs exhibit frequency-dependent leaky mode resonances[19]. Simulations on vertical Si NW arrays have predicted resonant peak shifts as large as 500 nm for diameter changes as small as 50 nm[20]. With highly tunable absorption possible, single semiconductor NWs have been used to construct UV and visible photodetectors (GaAs[21], ZnO[22], ZnS[23]). Other more complex devices such as Light Emitting Diodes (LED) and photovoltaics require p-n junctions within the semiconductor. While p-n junctions are easily formed from both top-down and bottom-up synthetic routes, top-down techniques are normally required to form functioning macroscopic arrays. The most common top-down method requires selective etching of a p-n semiconductor film resulting in a NW array connected to a degenerately doped substrate base. Contacting the resulting array is simple for both p and n doped regions of the device and minimal risk of forming short circuit paths during device fabrication.

Si NW field effect transistors (FETs) have been demonstrated for several biological sensing applications. By coupling oxide surface chemistry with controllable NW doping, Si NW FETs can operate as biological sensors without an applied gate voltage[24]. The high surface area to volume ratio allows the NW to operate similar to a FET depletion channel. Surface functionalization causes selective binding of biological markers. When biological markers are attached to the surface the result is an electric field that serves as a pseudo-gate bias; the bias in turn changes the conductivity of the doped NW. Order of magnitude conductance changes have been measured and were shown to be dependent on marker quantity and NW doping. Results are even possible in more complex arrayed systems; where n and p-type Si NW have been used in parallel to show both positive and negative changes from a single cancer marker[25].

Many NW devices have been constructed from both organized and random networks. For example, large scale sensors have been developed by aligning Si and Ge NWs on separate layers of polymer. These aligned NW films are then used to create flexible large-scale FETs[7], since the NWs exhibit less fracturing and mechanical stress than thin films. Arrays have also been used in energy applications such as doped Si NW photovoltaics[26, 27], or ZnO NW piezoelectric energy generators[28-30]. In these cases, semiconductor NWs are doped via diffusion to create an array of functional device elements or generate energy by mechanical forces due to Schottky barrier formation with the conducting electrode. While array devices have been developed, issues with ordering and connectivity still impede scale up and industry development, as discussed in Chapter 1.3.

1.2 Semiconductor Nanowire Growth Processes

Semiconductor NWs can be synthesized from two distinct processes: top-down and bottom-up. Top-down methods normally involve the etching away of material from a pre-

patterned substrate, which is often doped beforehand. The result is highly ordered crystalline NWs with controllable shapes and diameters. Top-down processes are well known for producing geometries inaccessible by bottom-up. Unfortunately, much of the substrate is sacrificed in the removal process and cannot be recovered. Bottom-up processes commonly involve the growth of NWs from seed catalysts deposited on a substrate. One such method for generating bottom-up NWs is by using chemical vapor deposition (CVD) to induce vapor liquid solid (VLS) growth. Since discovery in 1964 by Wagner and Ellis[31], VLS growth has been used extensively to grow semiconductor NWs including Si[31-33], Ge[34-37], III-Vs[38, 39] and II-VIs[40, 41]. A significant portion of research has focused on Si NWs and Si heterostructures[42], in part due to the ubiquitous use of Si in the electronics industry. Semiconductor NWs differ from metallic analogs because VLS growth allows for precise transitions between n and p-type doping, such as phosphorous (P)/boron (B) doping of Si, or Si/Beryllium doping of GaAs[43].

Since we focus on group IV, specifically Si NWs, two Si NW growth processes are reviewed briefly. VLS processes commonly begin with the deposition of nanoscale metal catalysts, (commonly Au, Al, and Cu) or annealing of a metallic thin film, which ripens into nanoscale catalysts of varying diameter. When Si precursor gas is introduced to the system containing metal catalysts at a temperature above the Si-metal eutectic point the precursor breaks down on the surface of the catalyst creating a liquid alloy, which becomes supersaturated as more Si is introduced. After supersaturation, the Si-metal liquid alloy will begin to crystallize out solid Si of diameter dictated by the initial catalyst, allowing for relatively precise diameter control during the VLS process[44], as shown in Fig 1.1a. Axially doped NWs can be formed by flowing dopant precursors, such as diborane (B_2H_6), phosphine (PH_3), and arsine (AsH_3) during

the growth process (Fig 1.1b). Removing the Si precursor after growth will cause the metal catalyst to solidify, ending the wire growth and leaving a metal tip on each NW.

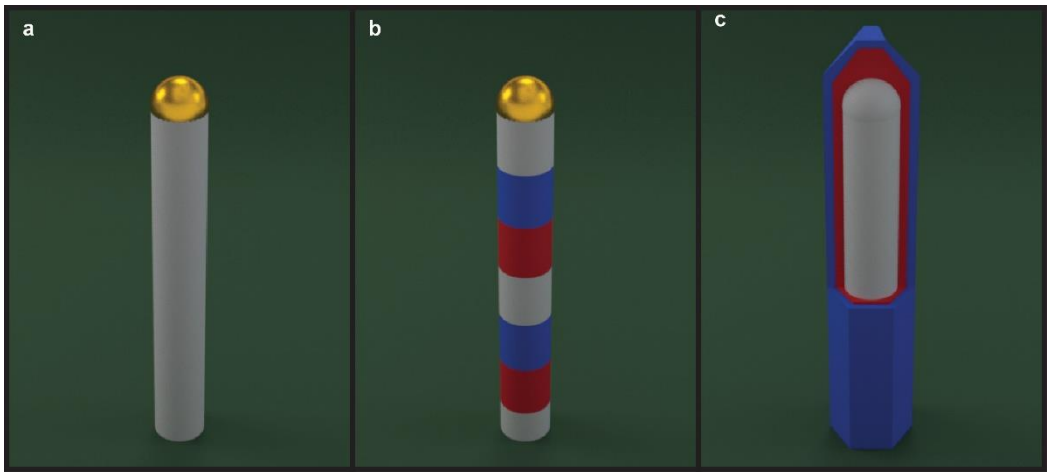


Figure 1.1| VLS and VS Illustration. (a) Undoped and (b) axially doped (i-p-n) Si NW grown via VLS with a gold catalyst. VLS NWs can undergo an additional (c) epitaxial VS process, presented here with a partial cross section (p-i-n), during which the gold catalyst forms an Au-Si liquid alloy and diffuses down the sidewall of the NW.

Epitaxial shell growth can create radially doped Si NWs (Fig 1.1c) at elevated temperatures far above the Si-metal eutectic. At high temperature, the Si precursor gas breaks down in the CVD chamber causing deposition on all surfaces, and epitaxial shell growth on Si NWs. Shell deposition for Si NWs can be crystalline, polycrystalline or amorphous depending on the temperature and pressure conditions.

Unless catalysts are templated on the growth substrate, CVD grown NWs are randomly oriented and distributed. Epitaxial growth is possible when the growth substrate is the same crystallographic orientation as the grown NWs. For example on a Si (111) substrate under the proper conditions, Si NWs will grow in the [111] direction, perpendicular to the substrate[45]. Even with vertical alignment many applications require ordered positioning on the growth substrate. One of the most common methods for alignment in NW arrays prior to growth is using predefined patterns generated from templates on the growth substrate. Electron beam lithography has been used to define precise patterns for catalysts on growth substrates, essentially serving as

a mask for gold deposition. While electron beam lithography can generate precise patterns, the time scale and overhead cost of the process precludes most industrial scale up. As an alternative to lithographically defined growth substrates, anodized aluminum oxide meshes (AAO) have been used as nanopore templates, which allow for ordered deposition of gold (Au) catalyst deposition, followed by VLS growth[46] or solution seeded synthesis[47]. The AAO pore size varies based on immersion time and anodizing voltage of the alumina layer, which allows for variable spacing and NW diameter, but a hydrofluoric acid etch is required after Si NW growth to remove the template from the structure[48]. Etching techniques, commonly referred to as top-down synthesis, have also been employed to generate ordered arrays of NWs[49-51]. Top-down techniques use both lithographically defined resists and ordered NPs to act as masks during the etching process. NPs will form an ordered layer on the surface of the sacrificial substrate, which can then be etched with Deep Reactive Ion Etching (DRIE) or wet chemical etch processes. Top-down synthetic techniques allow for precise control over doping, NW length and radius by changing the starting substrate, mask pattern and etch time. Since the sacrificial substrate is normally a pre-doped crystalline wafer, top-down synthesis results in a net loss of crystalline material to generate ordered NW networks. The precise control over spacing and crystallinity allows for the creation of anti-reflective light trapping surfaces tuned for visible light absorption[9]. Another important aspect is that ordering in both bottom-up and top-down synthetic regimes with electron beam lithography requires lithographic definition or ordered mask alignment of NPs prior to growth.

1.3 Nanowire Alignment Techniques

Without epitaxial growth and pre-patterned substrates, NWs normally grow along several different crystal directions and at random locations on the substrate dictated by the location of the deposited colloid. The disordered result of this growth process has led to the creation of several different alignment techniques. Since nanomaterials are vastly smaller than the scale where macroscopic industrial alignment practices can be used, other specialized methods have been developed. Unlike macroscopic alignment methods that commonly rely on mechanical positioning, NWs are often ordered using interactions with capillary and electrostatic forces in solvents[52]. One such collapse method drew inspiration from the liquid ring stains that occur during evaporation[53]. The evaporating ring method deposits patterned NWs at regular intervals due to slip and pin patterns of the evaporating solvent line[54], which can be modulated by changing the substrate, nanomaterial, functionalization and the solvent. While the spacing between deposition points can be varied, the NWs orient perpendicular to the moving solvent front and align end to end and thus are not as useful for semiconductor electronic applications where contacting specific doping regions are required.

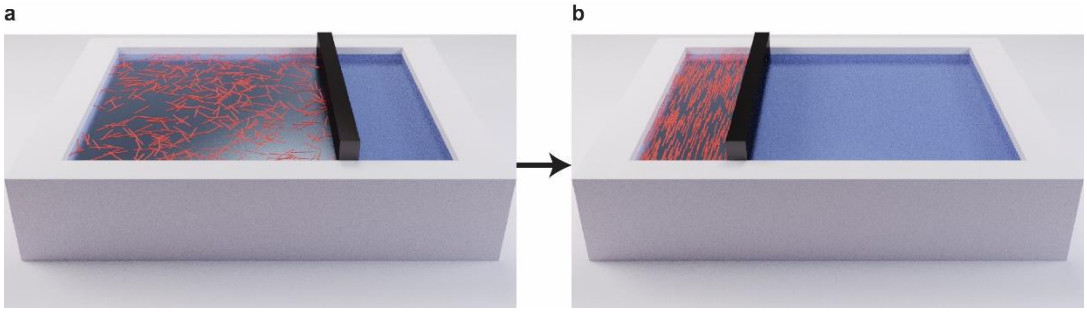


Figure 1.2| Schematic of Langmuir Blodgett Compression. (a) NWs (red) are randomly dispersed on the surface of the solvent in a Langmuir Blodgett trough (white). Parallel alignment **(b)** begins to occur as the free area is reduced with both NW-NW horizontal spacing and alignment angle changing based on the degree of compression.

Langmuir Blodgett (LB) is another common method for large scale aligned NW array formation. LB uses surface tension and NW surface functionality to trap deposited NWs at the

liquid/air interface. During compression the NWs will align generating the lowest energy superlattice[55] array (illustrated by Fig 1a). Modulating the hydrophobicity of the NW surface through functionalization ensures that the NWs reside at the liquid air interface. LB alignment has been studied with metallic NWs[56] since they are commonly synthesized with a solution mediated process, however, Si[57] and Ge[58] NWs arrays have also been created. In both cases the CVD grown semiconductor NWs are surface functionalized with a hydrophobic organic compound to avoid the formation of hydrophilic native oxide after exposure to air. While LB excels at generating parallel NW films with minimal angular variation, the NWs do not exhibit end to end linking, often generating large vertical gaps between adjacent NWs. Additionally, the high NW volume requirement is an impediment since NWs grown via CVD are physically connected to the growth substrate and difficult to consistently remove in high volume.

Other research has focused on ordering and collapse on the initial growth substrate. The capillary force between the NW and the substrate during solvent evaporation has been known to collapse vertical NWs, though the process is often unintended and uncontrollable, resulting in disordered aggregates of NW clusters[59]. To control this phenomenon, some have used lithographically defined half-moon pillars and collapsed using a controlled solvent evaporation technique[60]. The capillarity force on the flat side is reduced causing all pillars to collapse towards the half-moon side. The collapse could be influenced further by changing the direction of solvent evaporation across the substrate, which caused pillar collapse at different angles. While very useful for lithographically defined structures with identical geometry, non-epitaxial VLS growth can have variance in NW diameter, position, length and growth angle. Near neighbor NWs can exhibit additional capillary force causing collapsed NW clusters instead of a uniform NW array. Capillary action can be used in conjunction with alignment channels to precisely reorient NWs.

Evaporation of a NW solution will normally cause trapping parallel to the moving solvent front, as in the slip and pin method, but when microchannels are introduced the NWs will reorient perpendicular to the solvent front[61].

Contact printing, another common mechanical transfer method for deposited aligned NWs has been extensively studied for its ease of use and simplicity. The transfer process involves the contact of a NW donor and acceptor substrate followed by slow sliding motion. NWs on the donor substrate are transferred to the acceptor due to high friction and the large sheer force between the NW and the growth substrate[62]. Alignment and density of transferred NWs has been shown to improve by modulating the surface functionality of the acceptor substrate and by incorporating a thin oil layer between the substrates to reduce NW-NW friction[63]. Contact printing has been used to form heterogenous arrays by alternating the type of NW after each transfer. The array geometry can also be changed after transfer using lithographic or solvent mediated removal.

Stamp printing is another method for extremely precise transfer onto arbitrary substrates. However, it requires prior arrangement on the donor substrate beforehand, normally in the form of well-defined structures from e-beam lithography. In the stamp printing method varying peel velocities applied to a polymer stamp delaminate structures from a donor substrate (fast peel velocity) or adhere structures to an acceptor substrate (slow peel velocity)[64, 65]. Stamp printing has allowed for ubiquitous transfer of nanostructures and NW arrays, and can be coupled with other techniques, such as contact transfer, to move arrays onto arbitrary substrates with minimal loss. The resulting nanostructures can be transferred to flexible substrates to create robust transparent electronic devices or full devices can be fabricated prior to transfer to the acceptor

substrate[66]. Applications such as photodiodes[64], FETs[67], and TFTs[68] have already been demonstrated using the stamp transfer technique.

1.4 Previous Nanowire Welding Procedures

While proper order and alignment can generate precise semiconductor NW networks, connecting and accessing the network electrically has proven challenging. Generally these ordering methods create arrays where each individual NW must be accessed by separate electrodes using nanoscale lithographic patterning[7]. The missing element is inter-nanowire electrical connectivity, the idea that individual NWs are connected electrically to each other without the need of additional contact deposition. Inter-nanowire electrical connectivity allows for electrical contact on one NW to access the entire network similar to stick percolation. While methods for joining metallic NWs to form electrical connectivity have been studied extensively, there is little information on joining semiconductor NWs. Percolating films of metallic NWs have been used to create thin films with high conductance and transmittance[69-71]; two properties needed in the creation of next generation flexible touch screens and other flexible conductive media as demonstrated in Figure 1.3.

Metallic NWs as well as metallic carbon nanotubes (NTs) are commonly used as materials in percolation networks. Percolation normally refers to the point at which a randomly oriented and dispersed array of NWs will conduct from end to end. The critical density of NWs on a 2D square surface is dependent on the array area, the NW number and NW length and can be calculated through Equation 1-1[72].

$$n = N / \left(\frac{L}{l}\right)^2 \qquad \textbf{1-1}$$

Where n is the unitless density, N is the total number of NWs, L is the length of one side of the square array, and l is the average length of the NW. The critical density of n=5.64[73] was found for this simple stick percolation model, which considered electrical contact to occur when two NWs of negligible diameter intersected. This meant that for percolation to occur (on average) in any l x l sided area at least 5.64 NWs needed to be present. Many applications, such as touch screens phones, require a large fully connected conducting surface. For example, a capacitive 6 cm^2 touch screen (requiring 2 fully conducting 6cm^2 surfaces) would require at least 4 x 10^8 conducting NWs of length 10 μm. Unlike metallic NWs, which are normally spin coated to create a percolating network, collapsed VLS NW networks are three dimensional and thus cannot be approximated as all being in a single plane. While metallic NWs can be easily produced in large quantities through solution processing and several current welding methods reliably weld at inter-NW points of contact and avoid overall melting, expanding this process to semiconductor NWs is non-trivial. However, it is useful to examine past success at welding metallic NWs to set a basis for the welding of semiconductor NWs. Many different metallic NW welding methods have been developed often with a low resulting junction resistance (R_J), a literature review of the various welding methods for metallic NWs follows.

Metallic NWs are commonly formed through solution phase methods[74, 75], which can leave large organic ligands on the outer surface that acts as an insulating layer. For example, solution synthesized silver (Ag) NWs are often left with a surfactant coating of polyvinylpyrrolidone (PVP)[76]. While these ligand-terminated surfaces are ideal for impeding aggregate formation during growth, they act as a detrimental surface species post-growth and interfere with electrical conductivity between NWs within a network. Since organic species are

not difficult to remove at high temperatures a common method for forming Ag NW networks is through local heating.

Ag nanomaterial welding was first demonstrated by sintering spherical nanoparticles (NP). Sintering occurs when nanomaterials fuse below the melting point and therefore the particles do not undergo the liquefaction recrystallization process that occurs during the melting

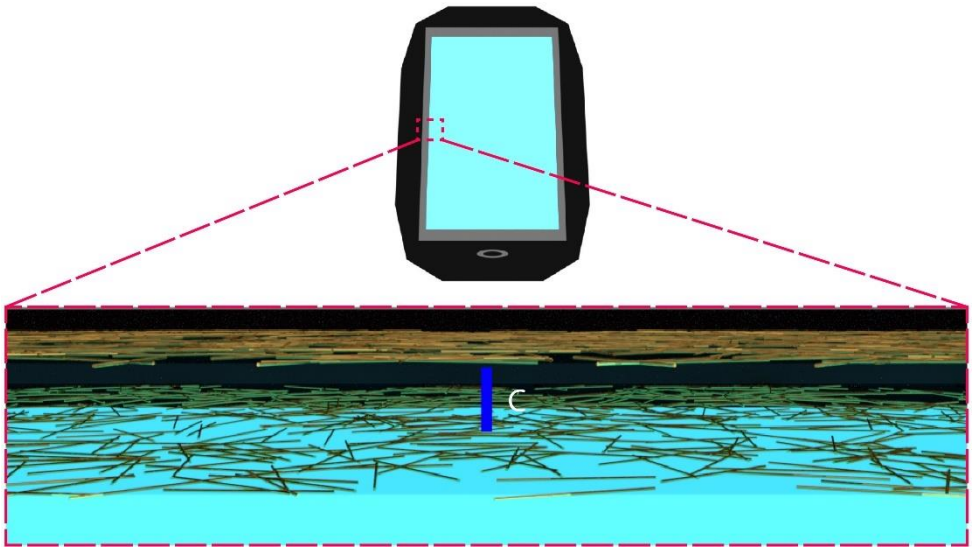


Figure 1.3|Metallic NW Touchscreen Operation. Schematic showing a perpendicular cross section of a touchscreen smartphone with two parallel metallic NW networks embedded in a transparent polymer mesh. The dark blue line and C represent the capacitive difference between the two networks. When the top network is touched C decreases which in turn signals an input at that location.

of NPs. Since perfectly spherical NPs have equivalent curvature at all points, surface instability/melting processes are less likely to occur at the sintering temperature. However, as temperature is increased beyond the sintering temperature, melting processes and agglomeration of NPs will occur. Several studies have indicated sintering temperature has a strong dependence on diameter as dictated by[77] Eq 1-2:

$$T_S = T_M\left(1 - \frac{\delta}{d}\right) \qquad \textbf{1-2}$$

Where T_S and T_M are the sintering and bulk melting temperatures, respectively, δ is a material parameter based on surface energy and atomic volume[78] and d is the diameter of the nanostructure. Equation 1-2 predicts sintering temperatures between 30 and 80% of the bulk melting point of most materials[79]. This phenomenon is also present for NWs, where sintering can occur at the intersection of two cylinders, where the geometry is similar to two adjacent spherical NPs. For example, annealing up to a maximum temperature of 300 °C (~30% of bulk Ag T_M) for 5 hours dropped the resistance by four orders of magnitude in a dense Ag NW network due to physical welding and junction formation between NWs[80]. However, thermal annealing of Ag NWs has also been shown to induce fragmentation and cause extensive structural changes at temperatures above the sintering point but far below the bulk melting point[80]. This diffusion process is known as Plateau-Rayleigh Instability, where atomic diffusion occurs until the structure is converted to the geometry of minimum surface energy. Plateau-Rayleigh instability has been demonstrated in in both metallic[80] and semiconductor[81-83] NWs as the tendency for cylindrical NWs to form regularly separated spheres at high temperatures. Since Plateau-Rayleigh instability can occur at temperatures as low as 380 °C for Ag NWs[80], it is important to find the ideal temperature that will remove the PVP surface functionalization and organic residue without reaching temperatures where the NWs will begin to break apart. The thermal annealing studies on metallic NWs indicate that while radiative heating processes can be used to generate targeted welding, the proper temperature must be found for each different diameter NW and can vary depending on material and growth conditions.

Since radiative heating can cause issues with instability and local heating/local joining methods dominate the macroscopic welding industry, much research has focused on finding low temperature solutions for joining metallic NWs. Illustrations in Figure 1.4 show several

processes that have been used to date in the low temperature welding of metallic NWs. Each method is normally employed with single crystalline metallic NWs that are synthesized via solution processing. Since no melting occurs in these regimes amorphous material is not present at the junction and grain boundaries are limited to regions where the weld forms.

Joule heating is a common phenomenon that occurs in resistors and electronic components. When electric current flows through a material, electrons scatter and transfer some energy in the form of heat. The current will then heat the area of highest resistance in the circuit, causing local heating. In NW percolation networks, each NW can be represented as an electrical wire with interwire points of contact being resistors as shown in Fig 1.4a. Since junctions begin with several orders of magnitude higher resistance than the NWs, a high amount of heat is generated at intersections within the network. As each weld forms, the overall network resistance decreases and the amount of joule heating is decreased, which allows for a self-limiting local heating process. While joule heating is an ideal local heating process, it often needs to be prefaced by a pre-anneal or pre-forming process since the starting junction resistance between the NWs can be over 100 MΩ due to surfactants. This high resistance means each junction acts initially as an open circuit, not allowing any current to pass through. Pre-anneal and electroforming are two common methods for pre-forming junctions before beginning a joule heating process[84]. Electroforming between Ag NWs has been shown to open migration pathways for charge conduction through the insulating PVP layers[76, 85]; and is also a common process for memristor design. Electroforming, unlike joule heating, causes atom migration across high resistance boundaries resulting in a lowered junction resistance without a physical change in geometry. After preforming, joule heating can be used to further anneal junctions (and in turn decrease junction resistance) while avoiding structural changes at other locations (such as NW

tips). Ag NW junctions with initial resistance of 560 Ω can undergo joule heating to reduce the resistance to only 30 Ω after ramping to 30 mV[84] with 5 mA of current passing through the junction. This equates to around 7.5 mW of local thermal energy generated via joule heating at the junction according to Joule's First Law: $P = I^2R$. Other NW joining methods draw inspiration from high pressure mechanical joining processes such as cold welding. Cold welding is commonly used in industry to bond two polished metal substrates. However, proper cold welding requires either extremely high vacuum and surfactant/oxide free surfaces or high applied pressures, though some research has indicated thin metal films can be welded at very low applied pressures when placed on elastomeric stamps[86]. The earliest example of cold welding metallic NWs was a proof-of-principle demonstration that welded two Au NWs, illustrated in Figure 1.4b. Au NWs were placed on the end of (Scanning Tunneling Microscopy) STM probe tips and manipulated using a piezoelectric stage and monitored in an electron microscope until welding appeared complete. While the two NWs formed reliable welds with minimal increase in junction resistance, some frictional force was required pre-weld to remove organic surfactants on the surface[87]. Additionally, this method requires complete control over the orientation and motion of each individual NW, making large scale network formation a challenge. Other mechanical welding methods, such as high-pressure bonding have also been scaled up to develop large scale networks at room temperature for integration into organic photovoltaics. However, applied pressures of 25 MPa for 5s were required for full welding throughout the network[88]. The high pressure, if applied slowly enough, can force all NWs into an extremely thin plane, roughly the height of the NW diameter. This is useful for generating thin flexible network electrodes for use as transparent conducting oxide (TCO) replacements, since the lowest possible thickness for many TCO films to retain functional conductivity is ~100 nm[89].

Plasmonic welding is a low temperature and low pressure method that has been developed for welding metallic NWs. Localized surface plasmons are generated in nanomaterials at resonant frequencies and propagate axially along the NW[18]. Plasmonic welding occurs when resonant frequency photons generate surface plasmons at the interface between aligned metallic NWs and air. The small nanoscale gap between NWs causes overlap in the electron oscillations from the surface plasmons, which in turn generates high energy local heating at regions where the NWs cross[90] regardless of NW orientation as shown in Figure 1.4c. The welds rely heavily on small <5 nm[91] gaps between crossed NWs to properly couple the surface plasmon and generate sufficient heat, meaning NW density must be high in the exposed region. Additionally, while many other joining methods discussed so far can be expanded to other materials like semiconductors by changing surface conditions, pressure and temperature, surface plasmon generation requires materials with high conductivity, which is one reason noble metals like Au and Ag are commonly employed.

Less research has been undertaken for welding semiconductor NWs. Unlike noble metals, semiconductors often have issues with problematic surface states, poor surface chemistry, in addition to significantly higher melting points, all of which impede the diffusion processes which drive NW welding. The inherent heterogeneity of semiconductors, both in doping and make-up, add difficulty when transferring metallic process techniques to semiconductors. However, some progress has been made in the welding of semiconductor nanomaterials.

Crystalline junctions are normally impossible, since crystallographic planes are randomly aligned during the welding process and melting processes will usually result in the formation of amorphous material. However, aligned growth has been used to avoid the issues with randomized orientation. Indium Arsenide (InAs) NW junctions have been formed by properly

oriented growth on Si substrates. Etching is used to create V shaped valleys in the Si, on which epitaxial growth of InAs occurs. The InAs NWs grow in the <111> direction, so any intersection between the NWs during growth results in a single crystalline, highly ohmic junction[92]. However, scale up and electrical testing normally require precise mechanical manipulation of the NWs.

Vacuum filtration has been coupled with heating to form percolating NW networks[71]. 'Nanonets' have also been formed by vacuum filtration[93] using VLS grown Si NWs. The vacuum filtration collapses all the NWs into a thin plane, which creates the initial electrical contact. However, without an anneal and etch step, the solution processing and ambient conditions create surface oxide, which drastically reduces the conductivity of the mesh. The nanonets produce μA currents at 5 V applied bias but also exhibit a Schottky barrier at low voltage.

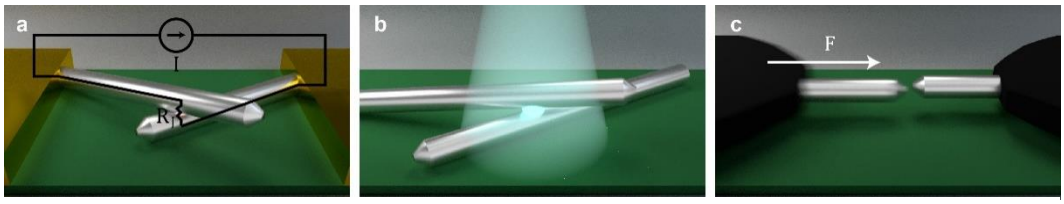


Figure 1.4| Metallic NW Welding Techniques. Schematics for three different metallic NW welding techniques. Joule heating (a) occurs when two NWs separated by a junction resistance (R_J) have a current flowing between NWs. The circuit diagram is overlaid on the schematic. Plasmonic welding (b) involves exposing crossed NWs to light matched to the resonant frequency to generate surface plasmons on the top NW. (c) Two movable probes holding Ag NWs. One probe is moved with proper force (F) until a weld occurs between the NWs. If F is too large NWs will be damaged or broken.

CHAPTER 2: METHODS

2.1 Chemical Vapor Deposition system construction

We constructed a home built CVD system to facilitate semiconductor nanomaterial growth that allowed for quick switching between precursors/dopants, a low operating pressure, quick output and advanced control over pressure/temperature ramping. The system was constructed with customizability in mind while adhering to strict standards for user safety.

All toxic gases, which consisted of electronic grade diborane (B_2H_6), phosphine (PH_3), silane (SiH_4), germane (GeH_4), were stored in gas cabinets (Matheson) so that catastrophic failure of the tanks would not result in toxic gas entering the breathing space. Less dangerous gases like hydrochloric acid (HCl), hydrogen (H_2) and argon (Ar) were stored in a walk-in fume hood that also contained the CVD system. Gas detectors (Honeywell) for H_2 and SiH_4 were placed in each gas cabinet and allowed close monitoring if any leak should occur. If a leak did occur the system was designed to trigger an alarm which would instantly depressurize all pneumatic valves leading to the gas tanks, stopping the process and allowing for immediate evacuation of the process line. All gas tanks were connected with diameter indexed safety system (DISS) gaskets, which offered an improved gasket seal compared to traditional CGA fittings.

The process lines leading to the system were made from ¼" 316 stainless steel (316 SS) tubing from Swagelok which was orbital welded and leak checked to 10^{-11} Torr. Since these regions regularly held 20 psi of toxic gas ensuring no leaks was prioritized. Other process lines (with less toxic gases) were added with Swagelok compression fittings and ¼" 316 SS tubing.

Carrier gases process lines also had .5 μm inline filters (Swagelok) to avoid outside contamination during tank replacement. The process lines led into mass flow controllers (MKS Instruments, PB4), which allowed precise computer control over each gas flow. By choosing a computer controlled mass flow controllers (MFC) we could change gas input, allowing for <1s transfer between n-type and intrinsic silicon, which was usedto create abrupt dopant regions on semiconductor nanowires. Pneumatic valves were placed after the MFCs for quick cut off of gas flow and to negate any accidental leakage through the MFCs after a gas change. The front manifold of the upstream system (Full System with description is show in Fig 2.1) was made from Swagelok VCR fittings, a type of threaded fitting where sharp internal faces seal on a metal gasket, which allowed us to add several process lines over a five-year peroid. The downstream part of the system also consisted of several pneumatic valves and an upstream bypass plunger valve, which allowed for direct purging of process lines during gas tank exchange procedures.

The actual growth process took place within a 1" bore tube furnace, in which we placed a quartz tube between two ultra-Torr fittings (Swagelok), which had been welded onto 2.75" conflat (CF) fittings. We found that the Ultra Torr fittings were important in maintaining a relatively low vacuum around 10^{-4} torr. Total pressure within the chamber was regulated through several valves. An automated butterfly valve (MKS, 253B) was used to regulate pressures between 0-20 torr via external connection to PC. For pressures between 20 torr and 100 torr a needle control valve (MKS, 148J) was coupled with a capacitance-based gauge, which measured the pressure of the upstream /growth chamber from .01 torr to 760 torr. A 60 μm inline filter (Swagelok) was placed in front of the needle valve to prevent debris build up without decreasing gas throughput downstream. A dry screw pump (Kashiyama SDE120TX) was used and regularly

reached base pressures around 10^{-4} torr. For pumping hydrogen and diluting toxic gases before exhaust a N_2 line was added and mixed with the process gases during the pumping process.

2.2 Growth of VLS nanowires

A home-built chemical vapor deposition (CVD) system was used for all syntheses and includes a quartz-tube furnace (Lindberg Blue M), H_2 and Ar carrier gases (Matheson Trigas; 5N semiconductor grade), and reactive gases (Voltaix/Air Liquide Advanced Materials) SiH_4, GeH_4(10% in H_2), and PH_3 (1000 ppm in H_2). NW growth substrates consisted of Si/SiO_2 wafers (Nova Electronic Materials; B-doped 1-10 Ω·cm Si wafers with 600 nm thermal oxide). For NW growth, substrates were placed in an ultraviolet/ozone cleaner (Samco UV-1) and functionalized with a 10:1 water: poly-L-lysine (0.1% in H_2O, Sigma Aldrich) solution followed by dispersion of citrate-stabilized Au colloids (BBI international) with diameters of ~30-100 nm. N-type Si NWs were grown in the CVD system following a modified literature procedure[94, 95] using a 5 min 450 °C nucleation step followed by a ramp (1 °C/min cooling rate) to 420 °C with 200 sccm H_2, 2 sccm SiH_4, 10 sccm PH_3, and a total growth time of 5 hours. NW arrays were collapsed by sliding the growth substrate directly from the quartz tube into liquid nitrogen (N_2) while flowing 200 sccm Ar. ENGRAVE NWs were grown via the same VLS process by modulating the phosphine flow on and off. Germanium VLS NWs were grown in the above system using 100 sccm of Ar, 15 sccm of Ge at 350 °C for 30 minutes followed by a temperature decrease to 260 °C for several hours with a process pressure of 300 torr throughout the growth.

2.3 Deposition of germanium thin films

Germanium thin films were deposited using a modified literature procedure[96]. Briefly, Si/SiO_2 wafers (mentioned above) were cleaned in an organic wash and UV/Ozone and placed in the

CVD system at 600 °C under 100sccm of H_2 flow and annealed for 10 minutes. The temperature was dropped to 350 °C after which the H_2 was removed and replaced by 60 sccm of Ar, 1 sccm of SiH_4, and 10 sccm of B_2H_6 at a chamber pressure of 20 torr. Afterwards, the chamber was evacuated and filled with 100 sccm of H2 and 10 sccm of GeH_4 at 5 torr and the temperature was dropped to 330 °C over 20 minutes and held at 330 °C for 1 hour afterwards, resulting in a nominally uniform poly crystalline Ge thin film of ~300 nm. After depositing the Ge film, the samples were taken to plasma enhanced CVD (PECVD; Advanced Vacuum Vision 310 Plasma Enhanced Chemical Vapor Deposition System) for deposition of a ~50nm surface oxide layer. An additional solvent wash and UV/Ozone cleaning followed before gold nanoparticles were deposited onto the surface. Growths that used these substrates underwent no additional modifications. Post growth, etching of Ge was completed in a bath of dilute hydrogen peroxide (Fisher Scientific 30%) warmed to a temperature of 50 °C.

2.4 Lithographic patterning

Marker patterns were written using Electron-beam lithography (EBL) and a Nanometer Pattern Generation System (NPGS) to transcribe a number and dot pattern developed in AutoCad onto a resist surface. EBL was completed using a FEI Helios 600 Nanolab
Dual Beam Electron Microscope with 5 nm scale resolution using an accelerating voltage of 30 kV and currents of 11 and .34 nA for large (written at 65x magnification) and small features (written at 100x), respectively. Si wafers with 100 nm thermal oxide and 200 nm Si nitride (Nova Electronic Materials) were cleaned and spin coated (Laurell Technologies Model WS-650-23B) with 2 layers of methyl methacrylate (MMA) (MicroChem MMA (8.5) MMA EL 9)

and 1 layer of poly-methyl methacrylate (PMMA) (MicroChem 950 PMMA A2). Each layer was spun at 4000 rpm for 30 s and annealed at 180 °C on a hotplate for 60 s.

After EBL, patterns were developed in methyl isobutyl ketone (MIBK) (MicroChem MIBK/IPA 1:3 Developer) for 90s and rinsed in isopropyl alcohol (IPA) for 60 s. 50 nm of Au was deposited via electron beam evaporation (Thermionics VE-100) at ~1 Å/s and a base pressure of 9 x 10^{-8} Torr. After deposition acetone was used to dissolve the PMMA/MMA layers and finish the pattern.

2.5 Registration and contact deposition

NWs were transferred via mechanical transfer by pressing the growth substrate and the marker substrate together and slowly pushing. NWs were imaged on markers in the FEI Helios SEM under an accelerating voltage of 5 kV, a working distance of 4 mm and a current of .86 nA. Magnification was kept at <1000x to ensure that damage to the NWs would not occur. Afterwards NWs were registered in custom coded Igor software which placed NW outlines on the marker pattern DesignCAD file. Afterwards contacts were drawn in AutoCAD on the same file and the sample underwent the PMMA/MMA layering process that was mentioned previously (Section 2.4). EBL was completed with the same settings, but with an additional alignment step that ensures accuracy of patterning on the marker substrate. Afterwards samples were immersed in buffered hydrofluoric acid (Transene BHF improved) for 10 seconds followed by two water rinses, an IPA rinse and nitrogen drying. Samples were placed in the e-beam evaporator to ensure the chamber would be at a pressure below 1 x 10^{-5} Torr within 5 minutes of the etch, to avoid native oxide formation. Once base pressure below 1 x 10^{-7} Torr was reached, palladium

(Pd) and Titanium (Ti) were degassed. 3 nm of Ti was deposited at a rate of .3 Å/s followed by 50 nm of Pd at .5 Å/s followed by an additional 100 nm of Pd at 1 Å/s. PMMA/MMA were then removed by rinsing the sample in acetone.

CHAPTER 3: ADDITIVE JOINING METHODS

3.1 Introduction

While a medley of methods exist for organizing Si NWs[52, 62, 63], few methods exist for electrically joining the NWs within an organized array. Bottom-up synthetic techniques such as metal catalyzed VLS and vapor solid solid (VSS) growth have been used to generate high density NW arrays of perpendicular Si NWs[97]. Radial growth is also possible through a VS process, where higher temperatures cause the gaseous Si precursor to break down at a high enough rate for surface deposition instead of targeted deposition at the liquid AuSi/solid Si interface. Both methods have been used to create radially and axially doped Si NWs with a high degree of precision[98].

Both VLS and VS growth methods can add material to already grown NWs. This added material could potentially be exploited to form inter NW junctions. However, before this can occur the orientation for the NWs must be changed so that close contact will occur during the additive process. Solvent mediated capillary collapse has been shown in the past to collapse nanostructures, albeit randomly[99]. We developed and explored two methods, VLS regrowth and shell joining and tested whether either was feasible for creating crystalline ohmic junctions between NWs. Both methods are illustrated in Figure 3.1; both process begin at the same start point and either undergo another VLS growth or a VS shell deposition. In the VLS regrowth process, NW ideally grow into one another to form a single crystalline junction. However, an intersection without grain boundaries would be unlikely without properly angled NWs, which requires a pre-structured

substrate and precise epitaxial NW growth, previously shown using InAs NWs[92]. The VS shell process requires a highly crystalline and uniform epitiaxial shell to form around collapsed NWs since the shared shell region between NWs will act as the junction.

3.2 Methods

Si NWs were grown via a previously mentioned VLS process (Section 2.2). Following growth, samples were collapsed in isopropyl alcohol (Fisher), followed by a BHF etch to remove surface oxide. The BHF etch was quickly followed with another IPA wash to remove any residual BHF and samples were dried under nitrogen flow. Afterwards, chips were reinserted into the furnace and underwent either an additional VLS process (for VLS regrowth) or VS shell deposition. The VLS regrowth process was identical to the previously mentioned VLS growth, but run for various growth times. For the VS shell process, the temperature was ramped to 750-850 °C under 200 sccm of H_2, at temperature the pressure was set to 25 Torr and the H_2 reduced to 60 sccm with an additional .15 sccm of SiH_4 added. Shell deposition thickness was modulated by varying process time. SEM images were taken on a FEI Helios 600 Nanolab Dual Beam Electron Microscope.

Photovoltaic devices were constructed from n-type VLS cores followed by p-type shell deposition. n-type cores were grown on SiO_2/Si substrates using 10 nm Au catalysts. Growth was completed at 450 °C and a chamber pressure of 40 Torr with flows of 60 sccm H2, .5 sccm SiH_4, and 5 sccm PH_3. n-type NWs were then collapsed outside of the vacuum using the IPA/BHF process listed above. Afterwards the growth chip was reinserted into the chamber and an epitaxial n-i-p shell deposition process was performed similar to the one mentioned above except with the addition of .75 sccm of B_2H_6 (PH_3) for p-type (n-type). The resulting p-i-n structure was

BHF etched and sputtered with a film of ~2 μm Indium Tin Oxide (ITO) using a Kurt Lesker PVD 75 with an In_2O_3/SnO_2 90/10 wt % target (KJLC). Afterwards the substrate was coated with Apiezon W wax (Apiezon) and allowed to sit in BHF for several days until underetch released the ITO/p-n sample. Afterwards the Apiezon W was removed from the sample with successive washes of Hexanes (Fischer Scientific) followed by a standard hydrocarbon removal process in the UV-Ozone. The resulting film was placed in the E-beam evaporator with a foil shadow mask and was deposited with 3 Cr/200 nm Au after a brief BHF etch to remove oxide. Afterwards the sample was placed on a patterned circuit board (PCB) such that the gold pad on the bottom of the sample was connected to a copper pad which extended from under the sample. Alternatively, devices were constructed by first underetching to release the sample from the growth chip followed by the same gold pad deposition stated previously. Afterwards samples were placed on Au patterned glass with an equivalent pattern to the PCB. Following this half of the sample was shadow masked (to avoid creating a short between the Au and ITO) and ~2 μm of ITO was sputtered on the surface of the chip after a brief BHF etch. I-V data for devices were collected with a Keithley 2636A SourceMeter in conjunction with two Signatone micropositioners (S-725) and probe tips (SE-TL).

3.3 Results

Both VLS regrowth and VS shell joined samples were inspected in the SEM and are shown in Fig 3.2. Regrowth samples exhibited some junction formation as shown in Fig 3.2a, however; it was unclear whether the level of joining was sufficient for electrical connection between the two NWs. In the majority of cases the regrown NWs would deflect into another growth direction upon reaching another NW, often kinking into a parallel growth direction (Fig

3.2b). This is not surprising from VLS growth dynamics, since the regrown NW is reaching a solid Si surface and the Au catalyst is already super-saturated from the decomposition of SiH_4 during the growth process. Therefore, it is unlikely for the catalyst to dissolve solid Si from the impacted NW. Kinking in Si NWs has been observed previously when changing the Si precursor or temperature[100]. Therefore, it is unsurprising that VLS regrowth NWs kink when the growth is restarted or when reaching a solid barrier.

Shell joined samples resulted in exclusively poly-crystalline shells (Fig 3.2c), a clear contrast from previously reported NWs with highly faceted single crystalline shells[101]. A visible

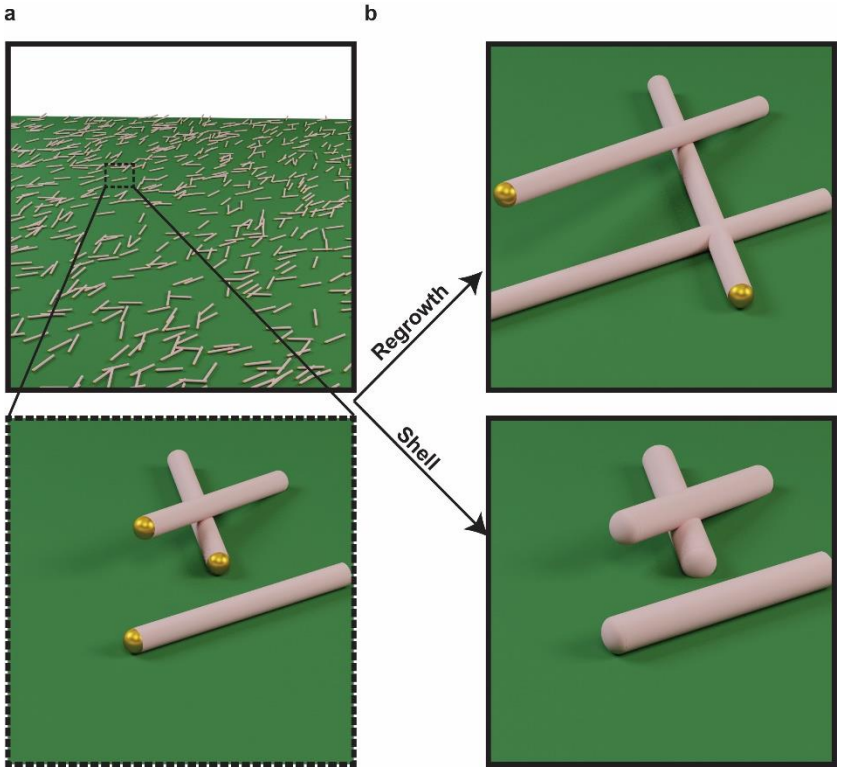
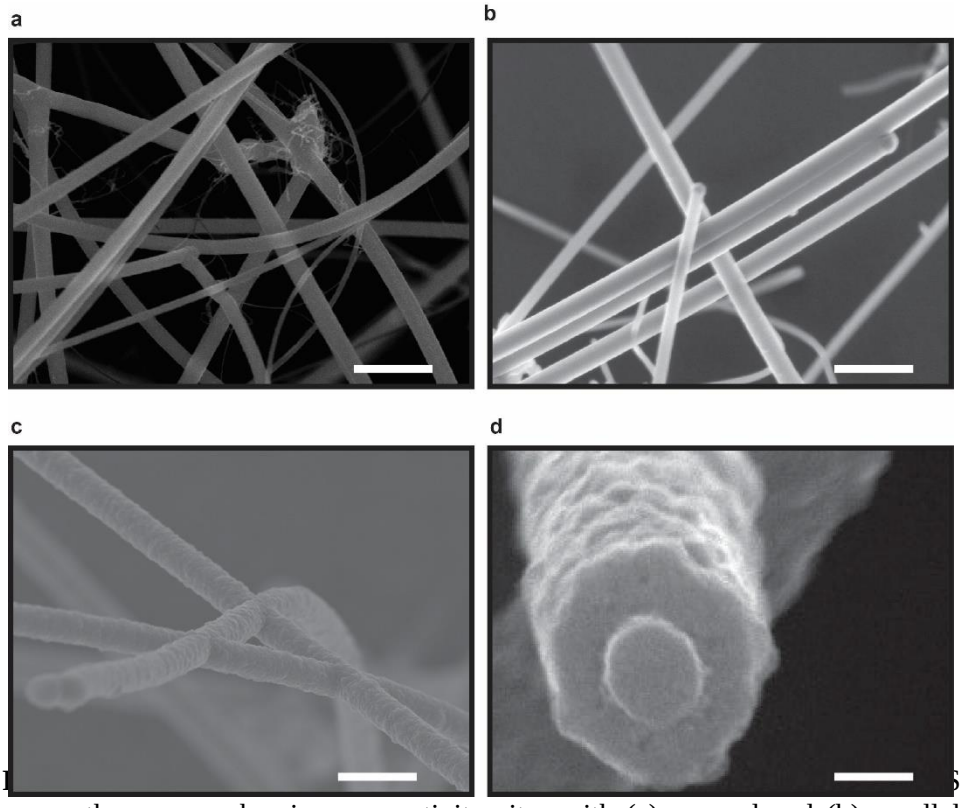


Figure 3.1| Additive joining method processes. (a) Schematic of collapsed, VLS grown Si NWs (top), and close up of NWs (inset). Illustration of the (b)VLS regrowth (top) and shell joining (bottom) process.

boundary was noted between the single crystalline core and poly-crystalline shell, shown in Fig 3.2d. While a junction was formed between NWs, the large number of grain boundaries in the polycrystalline shell would degrade the electrical properties of NWs, increasing the resistivity

due to the large number of defect sites[102]. Growing amorphous Si NWs and depositing amorphous junctions using VS was another possibility as amorphous Si (a-Si) NWs do have some benefits including a shell deposition temperature ~500 °C lower than the single crystalline and a much smaller required material depth for complete absorption, due to scattering at the disordered surface[103, 104]. a-Si NWs can also be grown in the solution phase[105] . However, amorphous Si is not ideal for percolation networks and electronic devices due to the large Number of defect states and lack of crystalline order. While the VLS regrowth result is not surprising, the shell result was unexpected. We have previously deposited epitaxial faceted single crystalline shells on Si NWs using an identical process as shown in Fig 3.3a. Since crystallinity



regrowth process, showing connectivity sites with (a) crossed and (b) parallel NWs; scale bars, 500 nm. (c) Shell joined NWs exhibiting connections at several points and the (d) cross-section of a 50 nm diameter crystalline core with polycrystalline shell, showing the clear boundary; scale bars, 1 μm and 50 nm, respectively.

normally increases with increasing temperature, we attempted another deposition was completed

at an elevated temperature of 850 °C which yielded silicon islands on the surface of the NW (Fig 3.3c) instead of a single continuous film. Silicon deposition on a clean Si-H surface should not have yielded any island formation at elevated temperatures during a homoepitaxial process; instead island formation indicated a heteroepitaxial process was occurring. The island formation was a sign of significant lattice mismatch between the NW core and the deposited shell[106]. At some point during the collapse process the surface of the NW was being oxidize, the thing native oxide causing a lattice mismatch during the deposition process. This has been studied previously for Si/SiO_2 heteroepitaxy, and can be estimated by lattice mismatch strain as per equation 3-1[107].

$$\Delta \equiv \frac{|a_d - a_s|}{a_s} \quad 3\text{-}1$$

where a_d and a_s are the lattice constants for the deposited material and the substrate respectively, and these values can be related to the critical thickness empirically according to equation 3-2[107].

$$t_c \approx \frac{a_d^2}{2|a_d - a_s|} \quad 3\text{-}2$$

Equation 3.2 is an empirical equation for the thickness (t_c) at which heteroepitaxy begins to form strain dislocations on the surface. However, since the native oxide formed on the surface of the NW is amorphous there is no way to find an accurate estimate. However, we can estimate the critical thickness based on the diamond cubic lattice of Si and the hexagonal lattice of SiO_2, which have lattice constants of 5.43 Å[108] and 4.90 Å [109] respectively, yielding a critical thickness of ~7.6 Å. However, the orientation of the SiO_2/Si interface has a large effect on this value as the

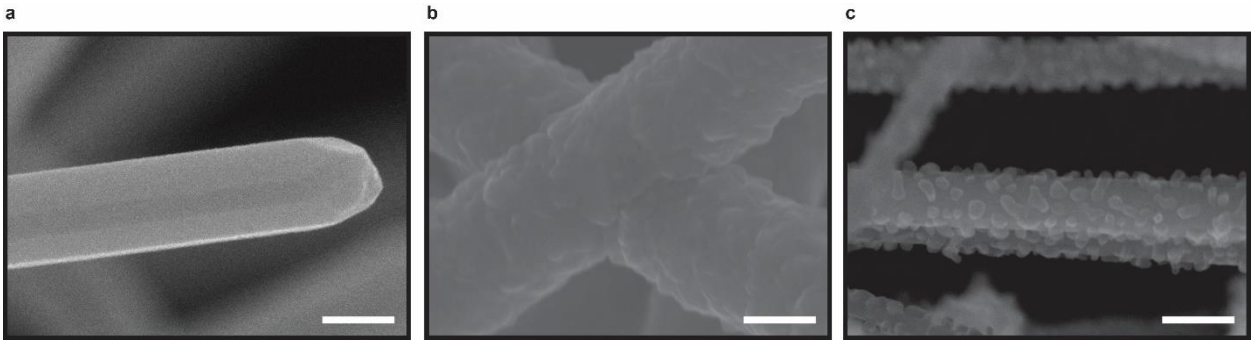


Figure 3.3| Shell Deposition Temperature. SEM images of NWs with shell deposited at 750 °C where cores were (a) never removed from vacuum and (b) removed from vacuum for collapse. (c) Shows the island formation from attempting the same shell process at an elevated temperature of 850 °C. Scale bars, 200 nm.

hexagonal unit cell of quartz has lattice constants of a=4.90 Å and c=5.40 Å. It is not surprising that amorphous native oxide would introduce additional strain and cause more dislocations in the deposited Si lattice. Since the NW surface did not show any signs of recrystallization and there is no inherent lattice mismatch between VLS grown Si and VS deposited Si, we concluded that the collapse process caused a small amount of native oxide formation on the surface of the NWs, possibly even sporadic coverage as low as 1-3nm, which prevented a single crystalline shell from being deposited.

Fig 3.3a and 3.3b compare the results of the previously successful VS shell deposition to the polycrystalline result that occurs with growth post collapse. In addition, island formation similar to the NW surface in Fig 3.3c had been previously reported in a study of Si agglomeration on silicon on insulator (SOI) substrates110, in which the authors concluded that Si aggregation was independent of oxide thickness. Therefore, even a small amount of native oxide of <5 nm could potentially disrupt shell deposition. Native oxide formation on Si-H surfaces in ambient environments is a known phenomenon111, and while the amount is non uniform and often <3 nm the formation can be near instant, especially for samples previously etched by fluorine112.

To test overall connectivity, n-type VLS cores with n-i-p deposited shells were created. Previous research has successfully created macroscopic Si micro-wire PV arrays by using VLS

grown n-type cores but required subsequent masking, etch and diffusion steps to finish the p-n geometry[113]. One of the most challenging aspects of creating NW solar cells was to create a barrier between the p and n-type contacts to avoid shorting through the device, which the authors do with a PDMS mask. Additionally, going from microwire to NW arrays would be challenging since polymers can have difficulty fully penetrating dense NW networks. We attempted to avoid shorting through the device by depositing the additional p-i-n shell on the NWs which created a corresponding thin film of ~200nm on the surface as shown schematically by Fig 3.4a. Contacts were deposited directly on n and p-type regions using sputter coating (top ITO contact) and e-beam evaporation (bottom Cr/Au contact). Fig 3.4b shows an example of a resulting PV device on a patterned glass substrate. Unfortunately, I-V data from each device was completely linear (as shown in Fig 3.4c) with resistance values of ~6kΩ.

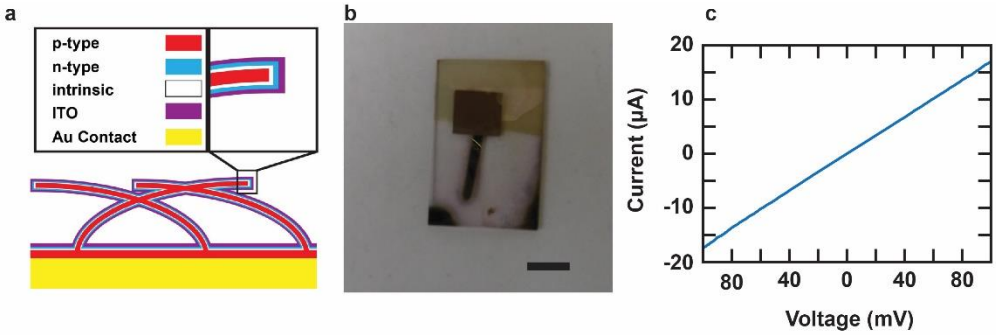


Figure 3.4| pin Device Construction. (a) Schematic illustration of the PIN NW/thin film device with an Au bottom contact and ITO top contact. (b)Photograph showing the discoloration from the sputtered ITO (light brown) which has been deposited on the upper 4/5 of the p-i-n device (dark brown) with an Au pad extending out from underneath; scale bar, 5 mm. (c) Linear IV data from a typical PIN device indicating the formation of a short circuit pathway.

Device construction was not possible without short circuit formation since I-V data reflected a resistor and the resistance was several orders of magnitude lower than expected from a polycrystalline Si device. Additionally, I-V data did not change when testing different regions on the film, indicating that a direct contact between the ITO top contact and gold bottom contact

was likely. Assuming the ITO film was relatively homogenous and continuous on the surface one contact between ITO and gold would be enough to short the device. The mechanical stress during the liquid etching process likely resulted in the creation of several short circuit pathways during contact deposition on the surface.

3.4 Conclusion

The results of the VLS regrowth and VS shell joining methods show the impediments of additive joining processes. While the additive methods yielded physical junctions between NWs, an important flaw was discovered in the methodology. Surface oxidation during the collapse process was highly detrimental to each joining method, as it acted as a barrier for crystalline deposition or regrowth. H-terminated surfaces are also highly reactive under ambient conditions and quickly form a stable oxide layer. The oxide layer can be removed with etching, but more control over the system is necessary to avoid future formation. The oxidized Si surface is so stable even a high temperature H_2 anneal could not change the surface functionality

Additionally, junctions did appear to form from VLS regrowth, but NWs would kink after impact. This kinking indicated that the growing NW was impacting a barrier and unable to graft material from the pre-grown NW onto the growing NW. Even without native oxide formation during collapse the VLS regrowth kinking would still occur. VLS grown NWs are supersaturated during growth and cannot draw material from a solid Si source, since the required diffusion process would not occur at a temperature ~30% of the melting point.

Devices consisting of p-i-n NWs and corresponding thin films were created to test the viability of the shell deposition method. Unfortunately, the I-V data from the resulting devices indicated that the underlying concept for the devices was flawed and resulted in short circuit pathways. In order to create devices from Si NW arrays it was clear that thin films (and therefore

shell processes) could not be used, since manipulating the films during etching/electrode deposition caused cracks.

CHAPTER 4: CAPILLARITY INDUCED SURFACE SELF DIFFUSION WELDING METHOD†

4.1 Introduction

Semiconductor NWs have seen usage in a wide variety of applications from electronics, photonics, energy, and biology[114, 115]. While device applications have been demonstrated using nanoscale proof of concept devices, further development will require integration on a macroscopic scale, potentially consisting of millions of accessible NWs. In order to generate large scale networks of NWs much research has focused on assembly and self-assembly techniques such as directed assembly[52], flow alignment[116], mechanical transfer printing[117], dip coating[54], electric-field assisted placement[118], and top-down patterning[119]. While these strategies excel at aligning NWs with precision, they normally require additional lithographic techniques in order to electrically access each individual NW in the array

For metallic NWs, electrically-active networks have been developed as a class of transparent and conductive percolating films with silver[120] (Ag), copper[121] (Cu), and gold[70] (Au) NWs, as well as metallic carbon nanotubes[122]. Ohmic connections between these components have been formed through a variety of techniques[123], including cold welding[87], plasmonic welding,[91] thermal annealing[80], mechanical pressure[124], diffusion bonding[125], and electron-beam induced welding[126]. In comparison to metallic NWs, however, semiconductor NWs could offer a wide range of advanced functionality by encoding field-effect transistors[127], p-n junctions[94], and

†Sections reprinted with permission from Celano, T.A. et al. Capillarity-driven welding of semiconductor nanowires for crystalline and electrically ohmic junctions. Nano Lett., 16, 5241-5246 (2016). Copyright 2016 American Chemical Society

memory bits[95] within the individual NWs of the network via in-situ doping[128].

Flexible meshes of silicon (Si) and germanium (Ge) NWs have been fabricated[129-133], but the structures are electrically-inactive or exhibit high junction resistances between NWs and non-linear current-voltage (*I-V*) curves across macroscopic percolation arrays[132, 133] as a result of insulating oxide layers or organic capping ligands on the NW surface. The formation of electrically-active connections between semiconductor NWs grown by a vapor-liquid-solid (VLS) mechanism has been limited to junctions formed either by electrical biasing individual wires,[134] patterning NWs to intersect during the VLS process,[135-137] or using a multi-step VLS process to create branched nanowires[138-140]. These strategies are generally limited to a low number of NWs and do not generate macroscopic networks. We demonstrate a capillarity induced welding technique that occurs 400-600 °C below bulk melting temperature that creates ohmic interconnects between semiconductor NWs.

4.2 Methods

Si NW were grown according to a previously reported procedure (Sec 2.2), VLS Ge NWs were grown using the same Si/SiO_2 growth substrate with a modified procedure. Ge NWs were nucleated for 30 min at 320 °C under 100 sccm Ar and 15 sccm GeH_4 (Air Liquide 10% in H_2) at 300 Torr followed by a ramp (5 °C/min cooling rate) to 260 °C and continued growth for 4 hours. Si NWs were welded in a range of temperatures from 815-875 °C and 100 nm Ge NWs were welded at 600 °C.

SEM imaging was performed using an FEI Helios 600 Nanolab Dual Beam system. Samples for HR-TEM and STEM were prepared by mechanical contact-transfer directly on to lacey-carbon TEM grids (Ted-Pella #01895). STEM imaging was performed on a Tecnai Osiris

operating at 200 kV with a sub-nm probe with a current of 2 nA (spot size 3, 4k extraction voltage). Drift-corrected STEM-EDS maps were obtained using the Bruker Esprit software. Acquisition time for each map was 15 min. STEM images were obtained before and after map acquisition to note any change in the sample.

For single-junction measurements, welded NWs were mechanically transferred onto devices substrates (Nova Electronic Materials; B-doped 1-10 Ω·cm Si wafers with 100 nm thermal oxide and 200 nm silicon nitride). Electron-beam lithography was used to pattern electrical contacts to individual NWs, and Ti/Pd contacts (3/200 nm) were evaporated in an electron beam evaporator (Thermionics VE-100) after a brief etch in BHF. I-V data for single welded junctions were collected with a Keithley 2636A SourceMeter in conjunction with Signatone micropositioners (S-725) and probe tips (SE-TL) or a Lake Shore Cryotronics PS-100 probe station.

4.3 Results

Au catalyzed VLS Si NWs were grown vertically then collapsed to be planar during the junction process. We immersed the collapsed network in liquid N_2 to avoid oxide formation during collapse, a schematic overview of the anneal process is shown in Fig 4.1. Liquid capillary force acting on the high aspect ratio NWs as solvent evaporates from the wafer[60] causes the NWs to collapse into a semi-planar network. A surface diffusion process is then used to weld NWs at each point of contact during a 4 minute process at ~400-600 °C below the bulk melting point of the material.

Ge and Si NWs were both grown using an Au catalyzed VLS process that avoids overcoating on the NW surface[95]. Si NWs were normally doped with phosphorous (P) to create

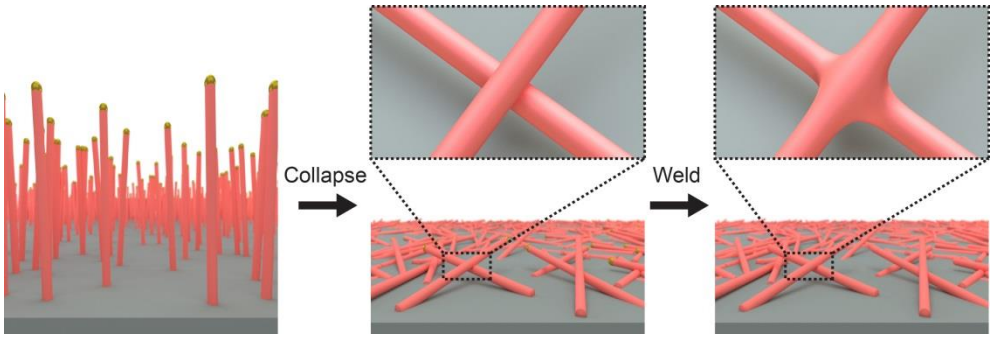


Figure 4.2|NW Junction Formation. NWs are grown through the VLS process, followed by a collapse and weld at temperatures ~400 °C below the bulk melting point. Insets show the morphological change typical before and after junction formation.

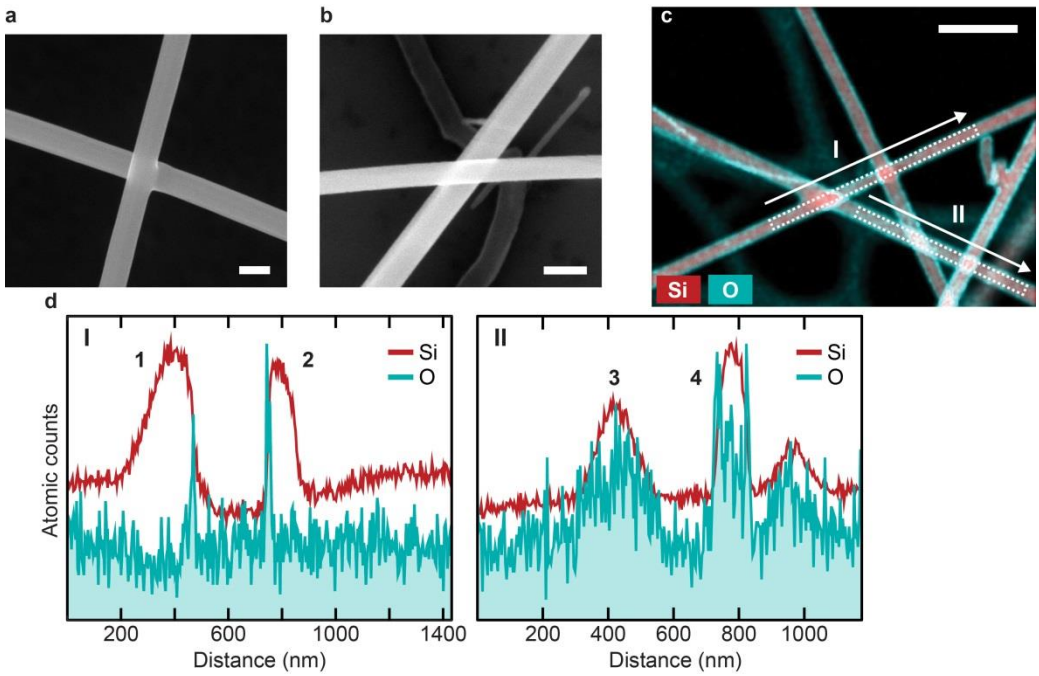


Figure 4.1|Comparison of welded and crossed NWs. SEM images of 100 nm diameter NWs that were (a) welded and (b) underwent the same anneal conditions with native oxide; scale bars, 100nm. (c) Overlapped EDS maps of Si and O showing two welded NWs (I) and two crossed NWs (II); scale bar, 500 nm. (d) Si and O line scans were performed on each dotted box region in the direction of the arrow.

degenerately doped n-type NWs and to minimize contact resistance during electrical measurements. NWs were collapsed in an oxygen free solvent (liquid N_2) to avoid the formation

of native oxide at contact points between NWs when the sample was removed from vacuum, which we had previously found was detrimental to junction formation (Sec 3.3).

We compared the SEM images of NWs which were collapsed in liquid nitrogen and those that were removed from vacuum for an hour after collapse to allow a 2-5 nm native oxide to form before welding. Fig 4.2a shows a typical perpendicular welded junction for NWs where no surface oxide was allowed to form. As a comparison, the sample in Fig 4.2b oxidized for several hours but also annealed at a 25 °C higher temperature to try to spur junction formation. However, no junction formation was observed. We preformed energy dispersive spectroscopy (EDS) to determine Si and O elemental maps within the NW network to determine the extent of Si/dopant diffusion and oxidation within the structure. Fig 4.2c shows elemental maps for Si and O for both welded junctions (I) and crossed junctions that are not welded (II). The normalized line scans of the elemental counts show the relatively flat O counts across the welded junctions 1 & 2 with narrow peaks indicating surface oxide formation on one side of each junction after completion of the welding process. Crossed NWs 3 & 4 show an O signal which tracks closely with the increase in Si indicative of the increase in native oxide surfaces one would normally expect for NWs that are crossed but not welded. HR-TEM and EDS elemental maps of Si, O and P for a degenerately doped Si NW display several features of junction formation (Fig 4.3). First, the HR-TEM image shows an increase in volume and area at the junction, creating a wider intersection than one would see if the NWs merely crossed. Secondly, the O map indicates surface oxide is absent from the junction connecting the two NWs. Third, the near two fold increase in Si signal at the junction indicates that no material is lost during the process and indicating a mechanism of diffusion rather than addition or removal of material. Lastly, since the

P elemental map has a close resemble to that of Si indicating that no dopant diffusion or aggregation is present at the junction.

The EDS maps and SEM images seem to indicate the junction is compositionally uniform and free of native oxide. Lattice resolved HR-TEM images further support this conclusion as shown in Fig 4.4. From the lattice resolved images we can make out the two single crystalline NWs that contribute to the junction. Additionally, since junctions occur regardless of intersecting angle between the NWs it is safe to assume that most junctions will not be single crystalline. However, from fast Fourier transforms (FFT) of regions on each NW we were able to confirm

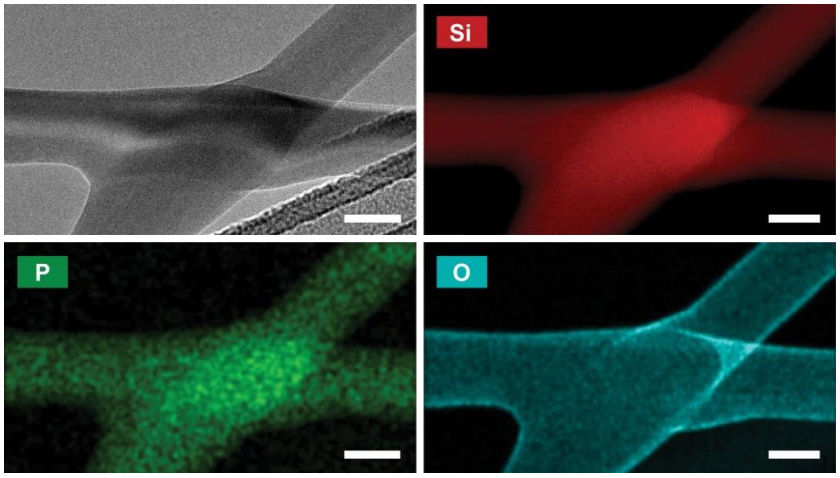


Figure 4.3|Elemental Maps of n-type Si NW junction. HR-TEM (top left) and EDS elemental maps of Si, P and O at the NW junction for an n-type Si NW doped at a level of 5 x 10^{20} cm^{-3}; scale bars, 100 nm.

the {111} lattice planes and the <112> growth direction (Fig 4.4b) using Equation 4-1[141]:

$$\frac{1}{d_{hkl}} = \frac{h^2+k^2+l^2}{a^2} \qquad \textbf{4-1}$$

Si NWs, like bulk Si, have a diamond cubic crystal structure with side $a = 5.43$ Å yielding a $d_{hkl} = 3.14$ Å, which is reasonably close to the lattice spacings of 3.14 Å and 3.28 Å calculated on each NW. Overall the junction appears to consist of single crystalline NWs with a grain

boundary at the point of formation, as shown by the single zig-zag grain boundary between parallel NWs in Fig 4.4c.

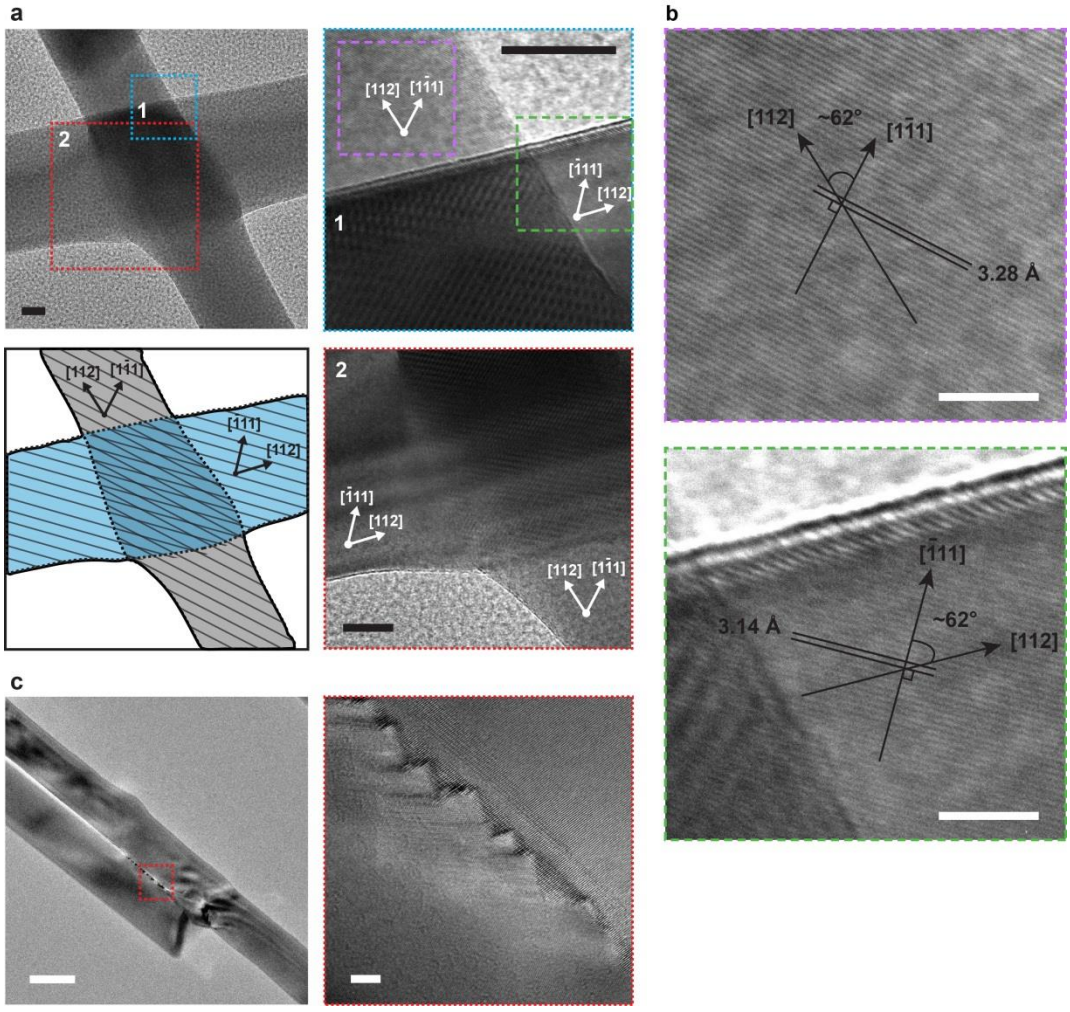


Figure 4.4|Determining crystallinity at NW junctions. (a) TEM image of a NW junction (top left), and a schematic showing the growth direction, {111} lattice planes and <112> growth direction of each NW; scale bar, 20 nm. Right, TEM images of regions 1 and 2 showing NWs on either side of the junction; scale bars, 20 nm. (b) HR-TEM lattice resolved images showing parallel {111} planes on each NW, spacing between lattice planes was derived from FFT transform data and growth direction was calculated from the angle between the lattice fringes and growth direction; scale bars, 5 nm. (c) Right: Welded single crystalline parallel NWs; scale bar, 100 nm. Left: HR-TEM image of red-box region showing a single zig-zag grain boundary between the two NWs; scale bar, 5 nm.

Temperature and diameter data was established through the qualitative visual assessment of SEM images of the junction and overall NW surface. A correlation between diameter and the

temperature at which the ideal morphological junctions formed was found (Fig 4.5a), and is shown in the SEM images (Fig 4.5b) of 100, 50 and 30 nm diameter NWs welded at temperatures that differed by 35 °C. From our qualitative assessment we discovered three regimes of distinct morphology. The first was the no structural change region (shown in blue), at which the temperature appeared to low for any visible morphological change to occur. The second was the structural instability zone (shown in red), which occurred at high temperatures where junctions began to break and the overall NW structure began to show signs of Plateau-Rayleigh instability as has been previously reported for Si NWs at high temperatures[81]. In between these two regions was the ideal welding condition (shown in green), where the only morphological change that occurred was the formation of the junction between NWs.

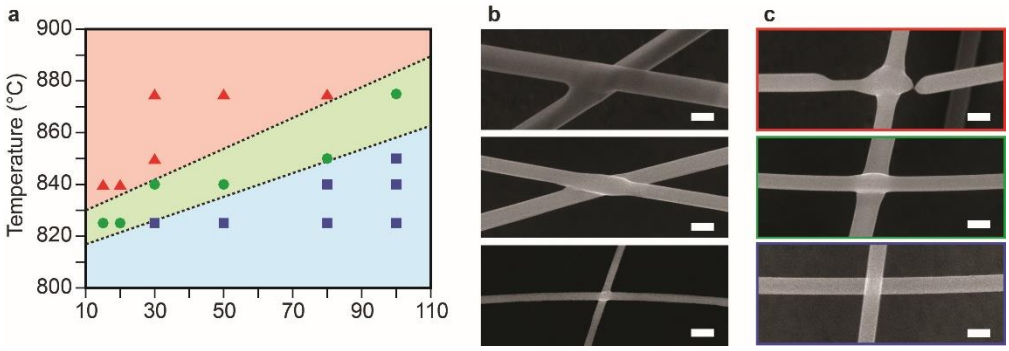


Figure 4.5|Temperature dependence on weld quality. (a) Qualitative chart of three different regimes for NWs welding, no structural change (blue squares), ideal weld condition (green circles), and complete structural instability (red triangles). Dashed lines and shaded regions approximate the difference between regimes. (b) SEM images representative of ideal welding for 100 (top) 50 (middle) and 30 nm (bottom) diameter NWs occurring at 875 840 and 840 °C, respectively; scale bars, 100 nm. (c) SEM images representative of structural instability (top), ideal welding (middle), and no structural change, for 80 nm diameter NWs at 875 850 and 820 °C, respectively; scale bars, 100 nm.

In general, these regions were found to be separated by ~25 °C evidenced in Fig 4.5c by the SEM images of 80 nm diameter NWs taken at 875, 850 and 820 °C. Ge NWs were also welded at 600 °C as shown in Fig 4.6, indicating that the process is expendable to different

semiconductor NWs. Increasing the time of the weld at ideal conditions seemed to have no further effect on the morphology (Fig 4.7) at or away from the junction, indicating that a self-limiting process was occurring at the junction. Reasonable increases in time did not cause regime changes like changes in temperature or diameter.

High temperature mass diffusion induced by local curvature has been studied for a

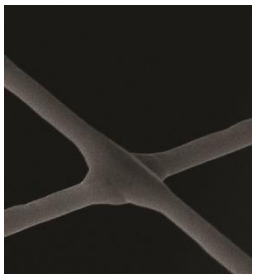


Figure 4.6|Ge NW Weld. SEM image of Ge NWs welded at 600 °C

variety of homogenous and heterogeneous systems[142]. Previous reports have determined as a general rule the diffusion temperature (T_D)is around 60-75% of the melting temperature (T_m)[142].

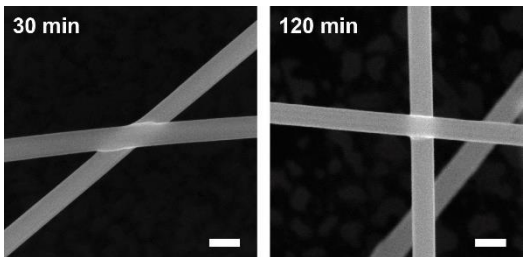


Figure 4.7|Effect of increased time on weld quality. SEM images showing the effect of increased weld time on 80 nm diameter NWs at an ideal welding temperature of 850 °C; scale bars, 100 nm.

This matches closely with the results we report in Table 4-1. We believe this method can be generalized to other semiconductor NWs and can be roughly estimated based on melting temperature and NW diameter.

Table 4-1| Comparison of 100 nm NW welding temperature (T_D) to the bulk melting temperature (T_m).

Material	T_m (°C)	T_D (°C)	T_D/T_m
Ge	938[143]	600	.64
Si	1414[144]	875	.60

We tested the electrical transport properties of the junction using a four point probe contact configuration on two welded NWs (Fig 4.9a). Si NWs were doped n-type with an encoded doping level of 2.5 x 10^{20} cm^{-3}.[145] The resulting I-V data was linear from -50 to 50 mV and the total resistance was used to calculate the junction resistance using Equation 4-4 and 4-5:

$$\boldsymbol{R_J = R_{exp} - R_s} \qquad \textbf{4-2}$$

Where junction resistance (R_J) is the difference between the total experimental resistance measured from the I-V data (R_{exp}) and the theoretical contribution of resistance from each single NW. The theoretical single NW resistance contribution is determined from the geometry of each NW measured by SEM according to Equation 4-5:

$$\boldsymbol{R_s = \rho\left(\frac{l_2}{\pi r_{1-2}^2} + \frac{l_3}{\pi r_{3-4}^2}\right)} \qquad \textbf{4-3}$$

ρ being the resistivity of the NW, which was measured to be .0018 Ω-cm from four point probe measurements on a single NW and matched previous reports[145]. l is the NW length from the innermost contact (2 or 3 on Fig 4.9a) to an established midpoint in the junction. r is the average diameter for each NW based on SEM measurements along the length. The values of each variable used to determine R_J are presented in Table 4-2. A value of 69 ± 4 kΩ is found for R_J which is comparable to an added length of 30 μm for an n-type Si NW doped at 2.5 x 10^{20} cm^{-3}. The ratio of junction resistance to resistivity is comparable to other reports of

thermal welding in Ag NWs[84]. Since R_J is likely independent of resistivity the resistance contribution from the junction should become irrelevant for lower doping levels.

Table 4-2| Variables used in the calculation of junction resistance.							
R_J (kΩ)	R_s (kΩ)	R_{exp} (kΩ)	ρ (Ω-cm)	l_2 (μm)	l_3 (μm)	r_{1-2} (nm)	r_{3-4} (nm)
69 ± 4	26 ± 4	94.5 ± 0.2	(1.8 ± 0.3) x10^{-3}	5.35 ± 0.03	4.69 ± 0.03	54 ± 2.5	43 ± 2.5

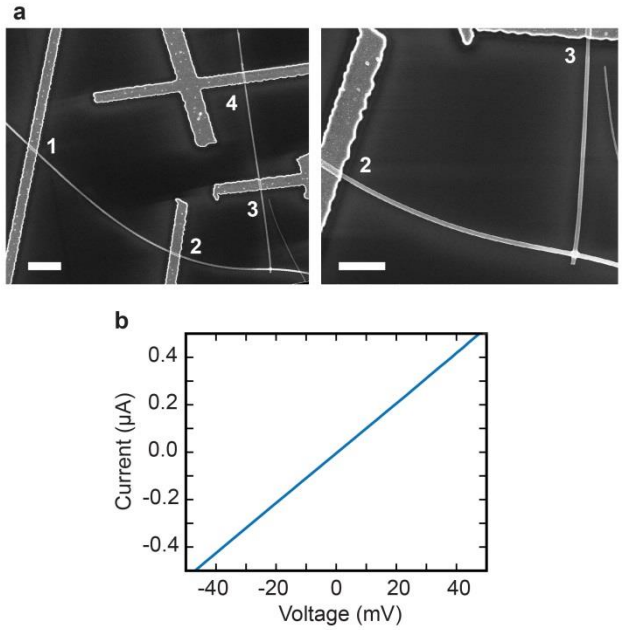


Figure 4.8|Single junction transport measurement. (a) SEM images showing the 4 point probe set-up for measuring the resistance contribution from the NWs and the junction(left); scale bar, 2 μm. SEM image showing the junction (left); scale bar, 1 μm. 4 point probe I-V data measured by sourcing current on contacts 1 & 4 and measuring the voltage between 2 & 3.

4.4 Conclusion

We succeeded in creating and expounding on a method for welding semiconductor NWs to form ohmic interconnects. While our efforts focused on Si and Ge, two common materials in the semiconductor industry, we believe that the capillarity induced surface diffusion process

identified here will be useful to a broad spectrum of semiconductors. The results match well with prior research on bulk surface diffusion indicating that connected NW networks can potentially be formed at temperatures lower than 60% the bulk melting point, regardless of material. Additionally, semiconductor NWs can have precise dopant profiles allowing for the specific tailoring of device structure in situ. The junctions generated by the welding process are highly crystalline and display no indication of dopant diffusion, meaning that any in-situ doping is retained at all locations, even at the junction. We believe this process may be useful for generating semiconductor NW networks and future research should be focused on welding NWs for specific device architectures as well as testing the generality of the process III-V and II-VI grown NWs.

CHAPTER 5: MODELING SI NW DIFFUSION AND WELDING

5.1 Introduction

Historically, welding materials has either been done with a process using melting, diffusion or some combination of both. Diffusion processes can occur due influences on the Gibbs free energy, which is affected by many different factors such as pressure, temperature, and chemical potential. Concentration and geometry create gradients in the chemical potential which serve as the driving force for the minimization of surface area for many diffusion processes. When coupled with applied thermal energy diffusion processes will occur over the chemical potential gradient until an energy minimum is reached. For example, cold welding, which has been used in metallurgy since the 14th century[86], occurs at room temperature but only under large applied pressures or tribological force. Many bulk diffusion techniques and phenomena have been expanded to nanomaterials to generate complex structures or vary size and geometry. For example, Au NWs attached to STM/TEM holders underwent a cold welding process joining them at the contact point when frictional force was applied[146]. PbSe quantum dots of various sizes have been synthesized from an Ostwald ripening process[147], which takes advantage of the fact that during mass transfer smaller islands will diffuse towards and "ripen" into larger islands.

Like Ostwald ripening, our NWs exhibited increased mass diffusion towards areas of high local curvature (NW ends and inter-NW points of contact).. We previously reported a temperature dependence (Section 4.3) on the welding process for different diameters of NW (different local curvature). Capillarity-induced surface diffusion, a process in which a change in

curvature creates a free-energy gradient that drives atoms away from areas of high curvature, is well-known to occur in spherical and cylindrical nanostructures[148]. The effects of this phenomenon include the blunting of W tips[149] and necking or sintering of nanoparticles[150]. To determine the role of this mechanism in welding NWs we modeled representative 3-D geometries of welded Si NWs. We developed three different models based on experimentally observed structures consisting of perpendicular, parallel and dissimilar diameter perpendicular welds.

5.2 Methods

The geometric models were created using version 2.70 of the program Surface Evolver[151] (Code for all surface evolver models is in Appendix A). The initial crossed NW geometry begins as a simplicial complex constructed from two perpendicular/parallel icosahedral prisms that intersect at four points to form a continuous body. The initial surface mesh is subdivided several times to increase the face count followed by a subdivision specifically targeting the long edges. After three subdivisions the surface undergoes several iterations of vertex averaging and equiangulation (normally until less than 500 faces are changed in equiangulation), which generates a more randomized surface to avoid errors and artifacts that occur when evolving an ordered surface. The surface is then allowed to evolve towards a minimal energy configuration via a gradient descent method under isochoric conditions. After each evolution a weeding step is done to remove small faces ($<1 \times 10^{-3}$) followed by vertex averaging and equiangulation. This process is repeated until the desired geometry is finally reached (all commands can be found in Appendix A). Geometries were exported as .stl files and imported as mesh into COMSOL Multiphysics and the surface gradient of the curvature was calculated with a weak-form boundary partial differential equation formulation. The surface velocity, v_s, was then calculated

as given by equations **5-1** and **5-2** using a value of $D_s(T)$ calculated from literature values for the Arrhenius expression, using a pre-exponential factor of 0.3 m^2s^{-1} and activation energy 2.5 ± 0.1 eV[152].

5.3 Results

The temperature and diameter dependence of the welding process that was previously reported in Chapter 4 indicated that a diffusion process may be occurring. In addition, the weld process occurs after a temperature ramp up with no added material, indicating a process of constant T, P and V, which is indicative of diffusion based on concentration gradient. The system was modeled using surface evolver, which minimized the surface energy calculated by the surface tension of the NW geometry. To understand the driving force behind the geometry change the diffusion process was simulated with each geometry. Diffusion is commonly understood through Fick's First Law. For the diffusion between dissimilar species Fick's First Law can be used to relate atomic flux to concentration gradient:

$$\boldsymbol{J = -D\nabla C} \qquad \textbf{5-1}$$

Where J is the atomic flux, D is the diffusivity constant and ∇C is the concentration gradient. Since we are dealing with a self-diffusion process, concentration gradient is not relevant. However, we can use the same equation structure to describe surface diffusion based on the relationship between chemical potential and surface curvature, as derived by Mullins[153]. The Young-Laplace equation describes capillary action due to changes in chemical potential on curved surfaces as follows:

$$\Delta\boldsymbol{\mu} = \boldsymbol{K\gamma\Omega} \quad \textbf{5-2}$$

Where $\Delta\mu$ is the change in chemical potential, K is the surface curvature, which in the case of a circular object is the inverse of the radius, γ is the surface tension, and Ω is the atomic volume. We can combine the Young-Laplace equation for chemical potential with the Nernst-Einstein relation, which relates the force acting on the species (F) to the drift velocity (v) of a species according to:

$$\boldsymbol{v} = -\frac{\boldsymbol{DF}}{\boldsymbol{k_BT}} \quad \textbf{5-3}$$

In our case the gradient of the chemical potential is the source of the applied force ($F = \partial\mu/\partial x$) yielding:

$$\boldsymbol{v} = -\frac{\boldsymbol{D}}{\boldsymbol{k_BT}} * \frac{\boldsymbol{\partial\mu}}{\boldsymbol{\partial s}} \quad \textbf{5-4}$$

And plugging Equation **5-2** into **5-4** yields:

$$\boldsymbol{v} = -\frac{\boldsymbol{D\gamma\Omega}}{\boldsymbol{k_BT}} * \frac{\boldsymbol{\partial K}}{\boldsymbol{\partial s}} \quad \textbf{5-5}$$

Where s is the arc length along the surface profile. By multiplying v by the number of atoms per unit surface area, which is equal to the $\Omega^{-\frac{2}{3}}$, we arrive at the equation for surface atomic flux J_s:

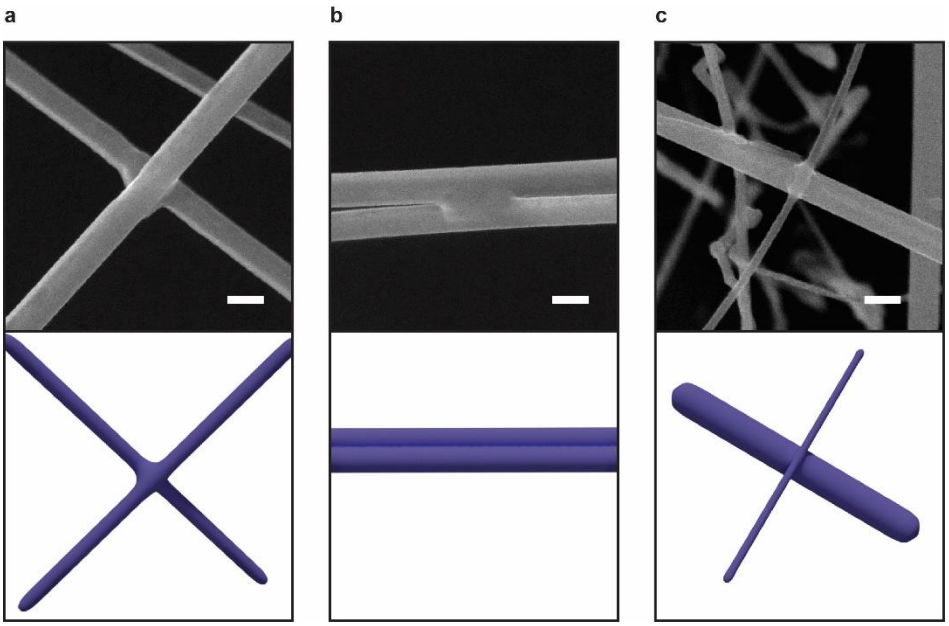


Figure 5.1| Characteristic Weld Types. SEM images (top) and surface evolver generated models (bottom) for three common types of welds during NW growth: (a) Perpendicular crossing, (b) parallel and (c) dissimilar diameter crossing. All scalebars are 100 nm.

$$J_S = -\left(\frac{D_S(T)\gamma\Omega^{\frac{1}{3}}}{k_B T}\right)\nabla_S K \qquad 5\text{-}6$$

For our example of two NWs in contact K is $(1/R_1+1/R_2)$ R_1 and R_2 are the principle radii of curvature, $D_s(T)$ is the temperature dependent surface diffusion coefficient, γ is the surface tension, Ω is the atomic volume, k_B is the Boltzmann constant, T is the temperature and $\nabla_s K$ is the surface gradient of the curvature. The velocity of the surface normal, v_s describes the deformation of the NW surface as it forms the junction, where positive and negative velocity manifest as increases or decreases in diameter, respectively. Dividing equation 5-6 by the number of atoms per unit surface area we can solve for the velocity of the surface normal:

$$\boldsymbol{v_s = J_s/\Omega^{-\frac{2}{3}}} \qquad \textbf{5-7}$$

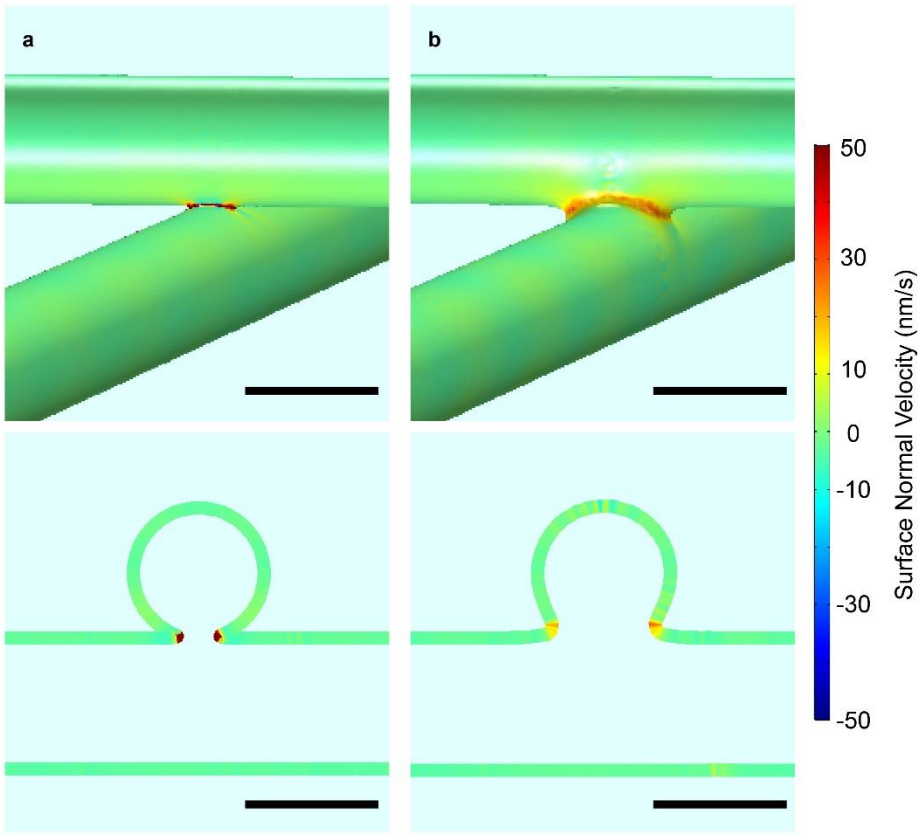


Figure 5.2| Crossed NW Simulation. Plots (top) show surface normal velocity at (a) initial and (b) midway stages of welding for perpendicular geometry NWs. Cross sections (bottom) show local maxima for surface normal velocity at the intersection between NWs. All scalebars are 100 nm.

Using Surface Evolver[151] and finite element calculations we generated models for each common type of welding between NWs as demonstrated by SEM images in Figure 5.1. Models generated in surface evolver were qualitatively assessed based on geometry when determining "initial" and "midway" points until reaching the final welded structure. The v_s for each stage of the welding process for both parallel and perpendicular NW junction orientations as seen in Fig 5.1.Figure 5.2 shows surface normal velocity plots for perpendicular 100 nm NWs during the initial and midway points of the junction formation at 850 °C. Surface normal velocity is solved using eqs 5-6 and 5-7 with a diffusion coefficient $D_s(850)$ of 1.8 x 10^{-12} m^2/s[152]. The cross-section images show that material diffuses to the regions at the junction to minimize curvature.

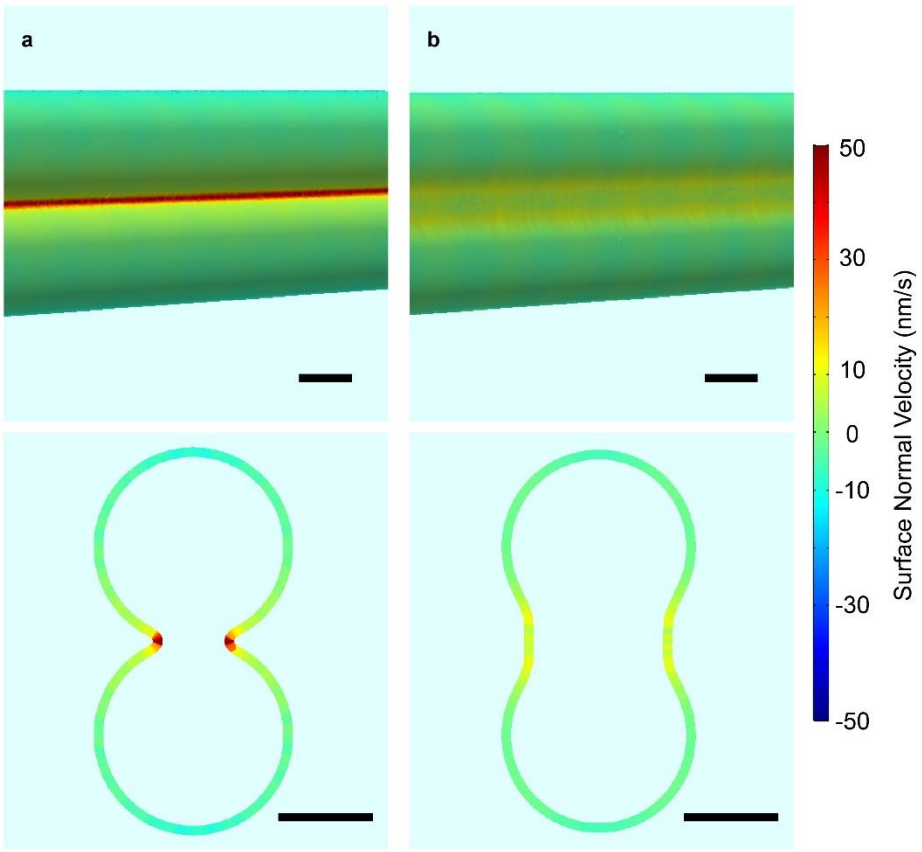


Figure 5.3| Parallel NW Simulation. Plots (top) show surface normal velocity at (a) initial and (b) final stages of welding for parallel geometry NWs. Cross sections (bottom) show local maxima for surface normal velocity at the intersection between NWs. All scalebars are 50 nm.

The junction contains the only significant region for diffusion at the ideal anneal temperature. Plateau-Rayleigh banding can be seen on the surface but occurs on a significantly longer timescale and with a significantly lower magnitude to the weld formation at ideal temperature. The structure of the instability bands is constant regardless of the extent of the weld and would likely be similar for any non-infinite cylinder. The initial maximum surface normal velocity at the junction is high at around 1244 nm/s, however at the midway weld mark, which shows a doubling of the diameter of the junction, the max velocity is only 56 nm/s. The sudden decrease indicates a self-limiting process is occurring at the junction and explains the lack of further structural change observed after ~4 minutes. Increasing the temperature above the ideal welding

temperature causes Rayleigh Instability bands to increase in intensity along both NWs as shown in Fig 5.4a. A single NW would undergo regular spheroidization at high temperatures, but joined NWs still have high surface normal velocity at the interface between NWs, which normally results in an aggregation at the junction at high temperature in addition to sphreoidization. The diffusion coefficient follows an Arrhenius equation, increasing by an order of magnitude when temperature goes from 800 to 900 °C, which helps to explain the small temperature range between ideal welding and surface instability.

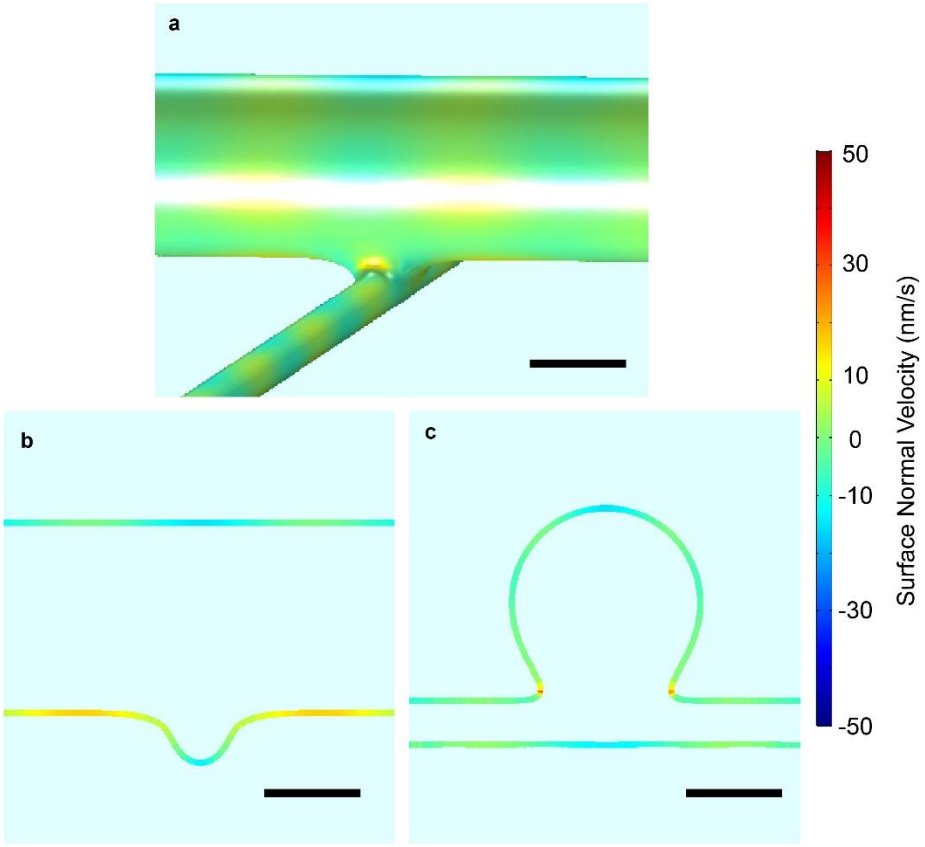


Figure 5.4| Mismatched Perpendicular Simulation. (a) Plot of surface normal velocity between 30 nm and 100 nm diameter NWs after weld formation. Cross sections show intensity profiles perpendicular to the (b) 100 nm and (c) 30 nm NW. All scale bars are 50 nm.

Parallel NWs show a similar trend with a sudden decrease in surface normal velocity from 56 nm/s to 18 nm/s between initial and final geometries as shown in Fig 5.3. The curvature quickly decreases when the two NWs are placed in parallel, and eventually a larger NW is formed from the two, which has been confirmed via SEM. This phenomenon often occurs when NWs collapse along a solution front leaving semi-circular patterns of parallel NWs. As the diameter of the NW is decreased it is increasingly common to find "welded" NWs that are double the initial growth diameter with a barely visible seam at the joining point. As temperature increases above the ideal weld threshold we often observe larger diameter NWs that do not undergo the characteristic spheroidization of Rayleigh Instability. The geometry drives parallel joining even at high temperatures of 950 °C, as shown by the lack of banding indicative of Rayleigh instability in Fig 5.5b. Through the weld process junctions can form across gaps as large as 5 nm so long as the NWs are in contact nearby.

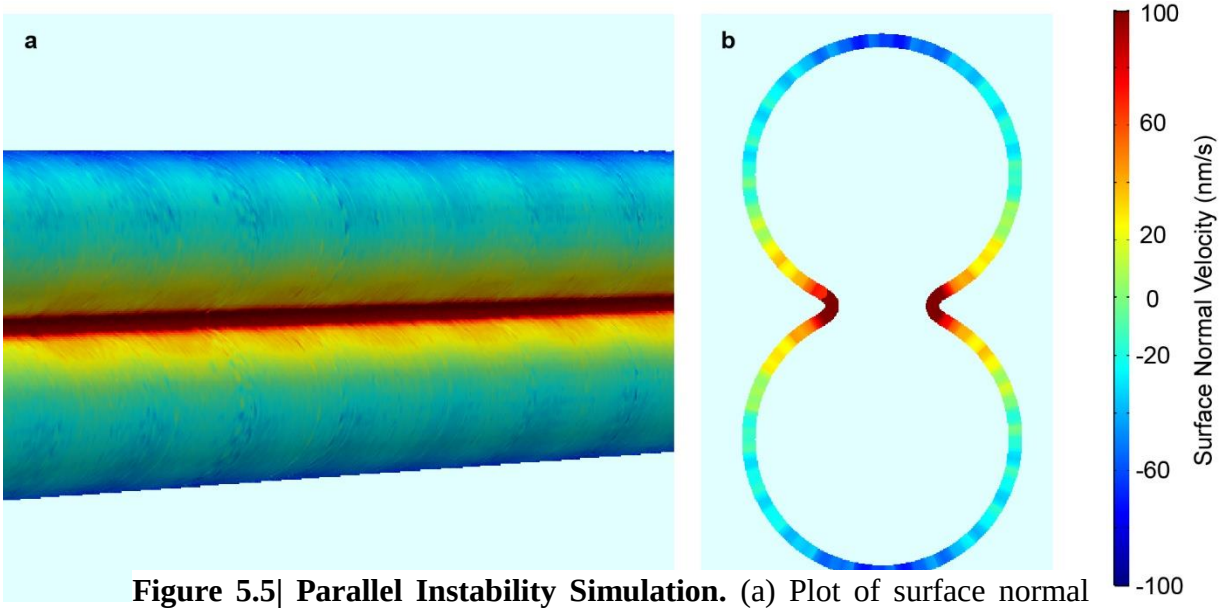


Figure 5.5| Parallel Instability Simulation. (a) Plot of surface normal velocity for parallel NWs post weld at 950 °C. (b) Cross section shows intensity perpendicular intensity profiles. Scale bars are 50 nm.

Junctions between NWs with dissimilar diameters, 100 nm and 30 nm, were also simulated. The initial decrease in surface normal velocity was the same as other simulated geometries, however the non-symmetric curvature drives the smaller NW to be consumed during the diffusion process and junction formation. Fig 5.4b shows a high positive surface normal velocity on the sides of the 100 nm NW and a large negative velocity on at almost all points on the 30 nm NW. Indicating the transfer of material to the larger NW. This is comparable to Oswald ripening, where smaller particles are consumed during the formation of larger aggregates. Increasing the temperature begins Rayleigh instability between the NWs as shown by the alternating surface normal velocity in Fig 5.6 which confirms our experimental results from section 4.3.

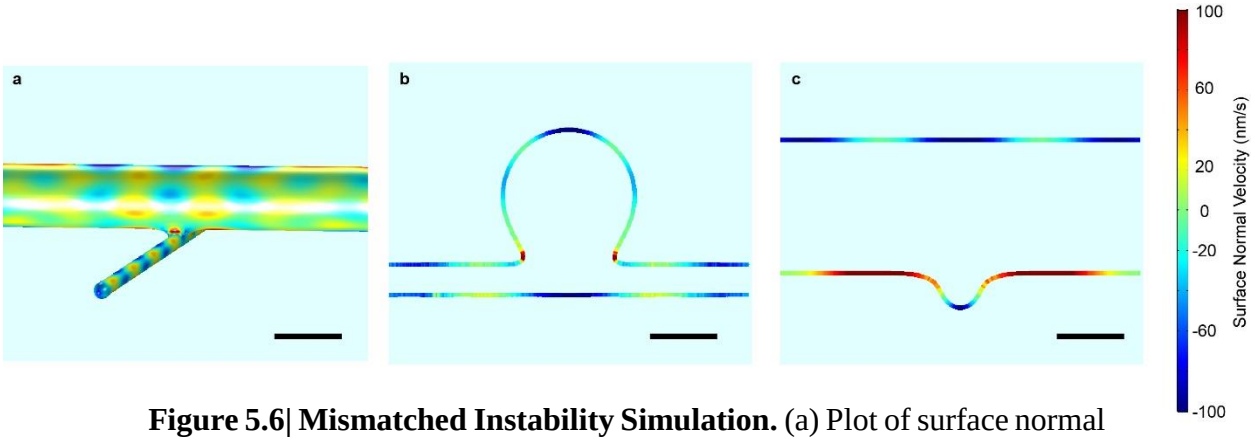


Figure 5.6| Mismatched Instability Simulation. (a) Plot of surface normal velocity between mismatched NWs post weld at 950 °C; scale bar, 100 nm. Cross sections show intensity profiles perpendicular to the (b) 100 nm and (c) 30 nm NW; scale bars, 50nm.

5.4 Conclusion

The welding mechanism was explained by capillarity induced surface diffusion, a process which is driven by large changes in curvature and high temperature but occurs below the bulk melting point. Multiple simulations were created to elucidate the nature of the capillarity induced surface diffusion mechanism for joining different NW geometries Different geometries showed

similar results, indicating that points of contact were maxima for the curvature gradient and in turn had the highest local surface normal velocity. The self-limiting nature of the junction was also demonstrated by the order of magnitude decrease in surface normal velocity between initial and final welding stages in the perpendicular NWs. Parallel NWs exhibited less Plateau Rayleigh instability, indicating the joining process that formed a large diameter NW was more likely than spheroidization at high temperatures. Perpendicular geometries exhibited Plateau Rayleigh instability which increased in magnitude as temperature increased and NW diameter decreased in accordance with previous experimental results. While making quantitative comparisons of surface normal velocities across different geometries are difficult due to the inherent qualitative weld progression from surface evolver, all simulations of capillarity induced surface diffusion matched well with prior experimental results.

CHAPTER 6: LARGE SCALE NW NETWORKS

6.1 Introduction

Semiconductor NWs have been used extensively in proof of concept device applications, demonstrating versatile applications on the nanoscale. Often the focus is on phenomena associated with the nanoscale size and geometry such as surface plasmon generation[154], memresistor switching[155], and photonic waveguiding. While each of these concepts has been generated on the small scale of several NWs, the full scale macroscopic integration of nanomaterials has proven to be challenging. Much research has focused on using metallic NWs as transparent conductors to replace the current transparent conducting oxides ubiquitous in the touch-screen electronics industry. While even highly degenerate Si will never be feasible for a touch screen TC, the same characteristics of high flexibility, transparency and connectivity are useful for biological, photovoltaic and electrical applications that require sensing or device complexity beyond a simple electrode. Both top-down and solution grown semiconductor microstructures have already been used for flexible electronic devices with applications including neural sensing[156, 157], energy storage[158] and energy harvesting[159]. Unfortunately bottom-up synthesized NWs similar to top-down NWs require lithographic definition or another form of patterning to grow ordered arrays. We disregard the disorder of bottom-up grown semiconductor NW array and study the electrical, optical and physical properties of the network.

We expanded on our previously reported mechanism for semiconductor NW welding by integrating connected NWs into centimeter scale devices. We demonstrate NW network electrode devices with regular macroscopic electrical conductivity over millimeter wide gaps and high optical transparency.

6.2 Methods

Nanowires were grown and welded using previously reported methods (Sec 2.2 and 4.2). The growth and welding process generated Si NW networks larger than 3 cm^2 on the growth substrate. Networks were also grown on Ge thin films (Sec 2.3) which acted as an underetch layer. Networks grown on Ge films were spin coated with polydimethylsiloxane (PDMS; Sylgard 184) at 1500 rpm for 30 s, and cured in a box furnace at 60 °C for 1 hr. The PDMS embedded substrates were placed in a diluted hydrogen peroxide (H_2O_2; Fisher Scientific, 30%) bath at 80 ˚C on a hotplate and etched for several days, depending on network area. After etching, freestanding PDMS NW networks were etched in BHF (Transene; Buffered Hydroflouric Acid) for 30 seconds to remove remaining silicon oxide.

Free standing PDMS embedded networks and growth networks were etched in BHF to remove native oxide on the NW surface and placed in an E-beam evaporator (Thermionics VE-100) with aluminum foil (Fisher Scientific, .018 mm thick) shadow masks with rectangular slits of 1 mm spaced 1.5 mm apart. At a base pressure of 1 $x10^{-7}$ Torr 3 nm of Ti and 200 nm of Pd were deposited at an average rate of 1 Å/s. Resistance measurements for free standing (flexed and straight) and growth substrate NW networks were collected using a Keithley 2636A SourceMeter in conjunction with Signatone micropositioners (S-725) and probe tips (SE-TL) or

a Lake Shore Cryotronics PS-100 probe station or a Lake Shore Cryotronics PS-100 probe station.

Voltage contrast images were collected in the SEM (FEI Helios 600 Nanolab) using the in-column secondary electron detector. Samples were prepared with lithographically defined contacts which were connected to a patterned circuit board (PCB; Injectorall, Patterns Printed via Pulsar Professional toner transfer package) using a wire bonder (West Bond model 7476D) with 1% Si/Al wire. One bond was made to the electrode connected to the NW network, and another bond was connected to the insulating substrate. The NW network electrode was connected to the SEM ground or a voltage source for passive and active voltage contrast, respectively. A bias of -20 V (+20 V) was applied to the NW network electrode for positive (negative) contrast.

Network transmittance spectra were collected on free standing PDMS embedded networks using a Microspectrophotometer (20/30 PV™ UV-Visible-NIR from Craic Industries) with a 50 x 50 μm aperture and 10x objective (Ultrafluor 10x 0.2 NA 7.4 mm WD) in conjunction with a halogen lamp source and CCD array detector. Backgrounds for transmittance spectra were taken from NW free PDMS regions on the sample less than 1 cm away from the network region to be measured. Diameter distributions for the 20/60/100 nm NWs were determined from 100 NW samples with diameters measured in the SEM.

Optical simulations were performed by Christopher Pinion using COMSOL Multiphysics. The two-dimensional simulation domain consisted of a Si NW with a circular cross-section placed in a vacuum encapsulated by perfectly matched layers (PMLs) to prevent reflection/scattering effects from the boundaries. Absorption characteristics of single NWs were simulated by impinging a plane wave with either transverse electric (TE) or transverse-magnetic (TM) polarization using the total-field, scattered-field method. A polarization-independent

transmittance was calculated by averaging the TE and TM transmittance. The simulation was repeated for NW diameters from 20-145 nm in steps of 2 nm. Simulation data was weighted for each diameter based on Weibull distribution functions for each diameter. The resulting simulation data was then adjusted such that the minimum and maximum transmittance matched the experimental result.

6.3 Results

VLS grown Si NWs were collapsed in liquid N2 and annealed (Fig 6.1a,b) at a temperature between 815-875 °C depending on diameter, based on previously reported data (Sec

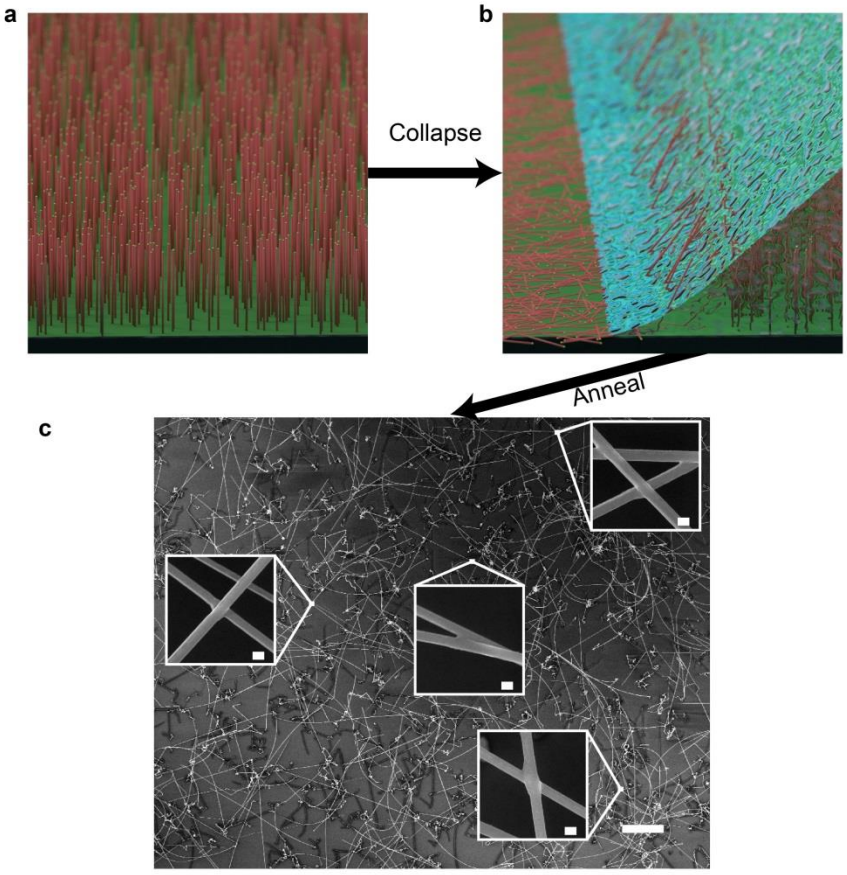
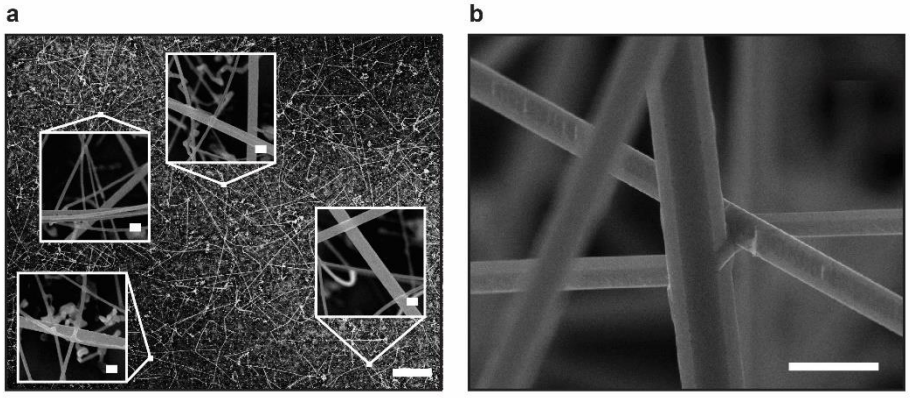


Figure 6.1| Macroscopic NW Networks. The overall process for generating large scale NW networks, an (a) initial VLS growth is (b) collapsed in liquid N_2 followed by an anneal process that yields millions of NWs in an (c) interconnected network with junctions formed at points of contact between NWs; scale bar, 10 μm, inset, 100 nm.

4.3)[160]. Liquid collapse placed NWs in close contact, which increased the number of junctions between NWs in the network. The resulting sample was a 6 cm^2 growth substrate with a network of NWs welded at each point of contact (Figure 6.1c). Density was controlled by the amount of Au catalysts deposited on the surface, with different dilution leading to colloid densities of 4 x 106, 4 x 107 and 4 x108 particles/cm^2 for 100, 60 and 20 nm NWs, respectively. In addition to uniform diameter networks, samples with different diameters were grown and annealed at the lower diameter anneal temperature. Figure 6.2 shows the resulting network of a mix of 30 and 100 nm diameter NWs annealed at 825 °C to avoid full instability of the 30 nm NWs. The



smaller diameter NWs formed junctions with each other and the larger diameter NWs, which

Figure 6.2| Dissimilar Diameter Welding. (a) 100 and 30 nm mixed network. Insets show welds between 30 and 100 nm NWs. Scale bar; 10 μm, inset 100 nm. (b) Example of 200 and 400 nm NWs welded at 900 °C. Scale bar; 500 nm.

indicates we can modify the overall architectural and electrical structure of the network without raising the temperature. Fig 6.2b shows a 200 and 400 nm NW welded at 900 °C, a temperature that according to our prior experimental model, should barely cause any change at a 200 nm junction, instead we see significant welding. This also implies that NWs could potentially be welded to planar surfaces such as thin films as the change in curvature is still significant between the flat surface and the NW cylinder.

We varied our networks by both diameter and density and noted that even at significantly higher density, smaller diameter NWs had a drastically lower collapse height of about 5 μm (Fig 6.3b). During evaporation, neighboring NWs cause lateral force perpendicular to the long axis of the NW causing them to bend towards one another. As the NW bends, downward axial forces parallel to the long axis collapse the structure towards the surface of the substrate. Due to the randomized nature of our colloid deposition and variation in diameter our nanowires exhibit a random collapse and connectivity pattern reminiscent of a non-ordered percolation network. Since NW location and diameter is variable, capillary force between neighboring structures is impossible to determine precisely. Though it is assumed that increasing the density would decrease the collapse height due to NW-NW interactions. However, by assuming equal force distribution and modeling the NW as a cantilever beam anchored at the base and undergoing deflection we can qualitatively assess why smaller diameter NWs collapse into a much more compact mesh using Eq 6-1[161]:

$$\emptyset = \frac{FL^3}{6EI} \qquad \textbf{6-1}$$

Where $\emptyset$ is angle of deflection in radians, F is the force acting on the NW perpendicular to the length L, E is the Young's Modulus and I is the moment of inertia, which can be related to diameter d by:

$$I = \frac{\pi d^4}{64} \qquad \textbf{6-2}$$

Moment of inertia increases with NW diameter, causing a decrease in deflection angle and overall lower collapse height. Growth rate is independent of diameter, NW lengths are equal, and the capillary force acting on the NW should be equivalent as material and solvent are the same

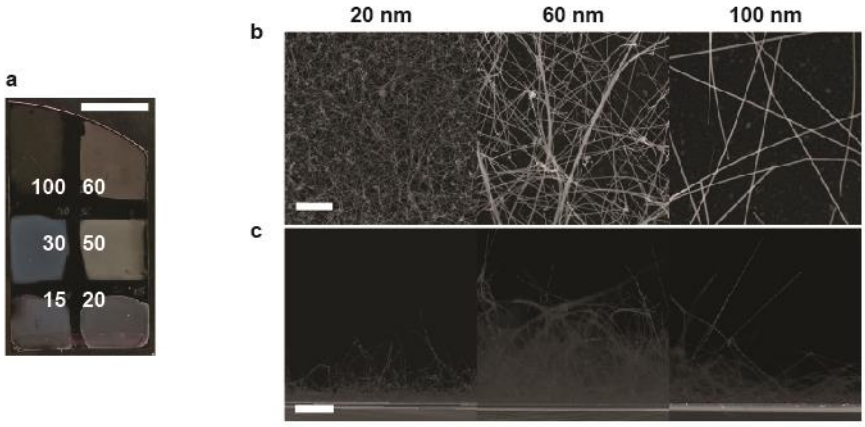


Figure 6.3|Diameter & density variation. (a) Photograph of a multi-section growth chip with NWs of various densities; scale bar, 5 mm. SEM images show both the relative densities (b) and collapse heights (c) for NWs grown with 20, 60 and 100 nm colloid; scale bars 1 μm (top) and 5 μm (bottom), respectively.

during each collapse. As moment of inertia increases the deflection angle decreases, which means that smaller NWs will deflect more, leading to a lower collapse height for the network. We reproduced this experimentally in Fig 6.3, where 20, 60 and 100 nm networks were grown on the same chip and compared in both collapse height and density, which were determined by the number of distinct NWs passing through five random regions in each sample. As expected from the initial deposited colloid concentrations of 7.0×10^{11}, 2.60×10^{10}, and 5.6×10^{9} catalyst/ml experimental densities of 81, 3.2, and .25 NWs/μm^2 for 20, 60 and 100 nm catalyst networks, respectively. Even though 20 nm networks had a density >20 times higher than the 60 nm network, the average collapse height was 3 times smaller. The trade off with collapse height between density and diameter is further evidenced by the slight increase in the collapse height when comparing the 60 nm to 100 nm section. Though it is worth noting both have outlier NWs which protrude from the main network by an additional ~10 μm. For applications requiring networks with smaller overall height, decreasing the density for the smaller diameter samples should yield better results. In addition, collapse height was often decreased further when the

samples were spun with a polymer or infiltrated with another material, due to either capillary force from another evaporation step or downward pressure during infiltration.

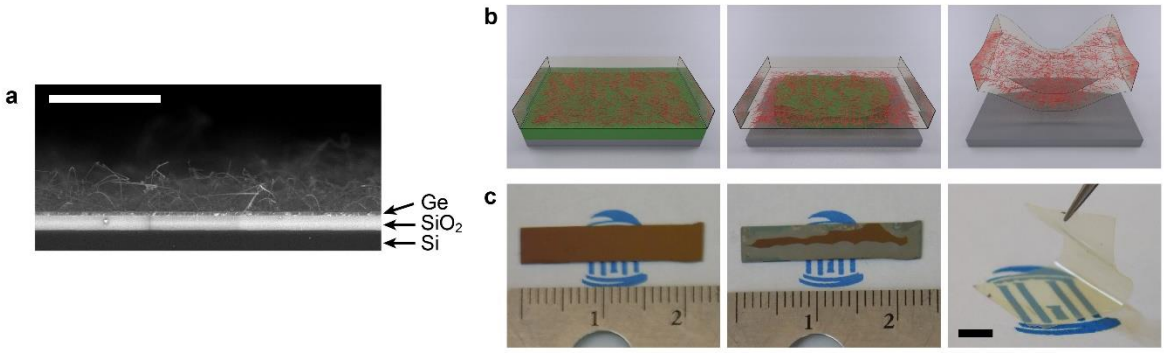


Figure 6.4| NW Collapse and Lift Off Processes. (a) SEM image of a collapsed 30 nm NW network welded on the surface of a sacrificial Ge layer; scale bar, 5 μm. (b) Schematic showing the Ge underetch and PDMS embedded network lift off process, beginning with the network embedded in PDMS (left), slow Ge underetch process (middle) and the resulting free standing flexible network (right), and (c) corresponding photographs, resulting PDMS embedded networks were 5-15 μm thick; scale bar 5 mm.

Networks were also removed and placed on arbitrary substrates by encasement in PDMS as shown in Fig 6.4. Briefly, a layer of ~200 nm thick Germanium was deposited before growth and acted as a sacrificial layer after the network was formed. Germanium was selected as a heat resistant material that would survive the high temperature (>800 °C) anneal. Additionally, the etching of germanium with H_2O_2 avoided the use of harsher etchants, such as hydrofluoric acid that caused damage and degradation to the NWs over the multi-day etch. NWs were then infiltrated and spin coated with PDMS. Ge was under etched in a H_2O_2/H_2O solution over the course of several days to release the fully embedded network as shown in Fig 6.4c. Required etch time could be decreased by increasing Ge layer thickness, as a larger layer would allow better exchange of aqueous reacted Ge at the solution/Ge interface. The resulting polymer embedded network was highly transparent and flexible. Previous research has focused on the relationship between NW diameter and the optical resonant response. Lorentz-Mie scattering[162] has been

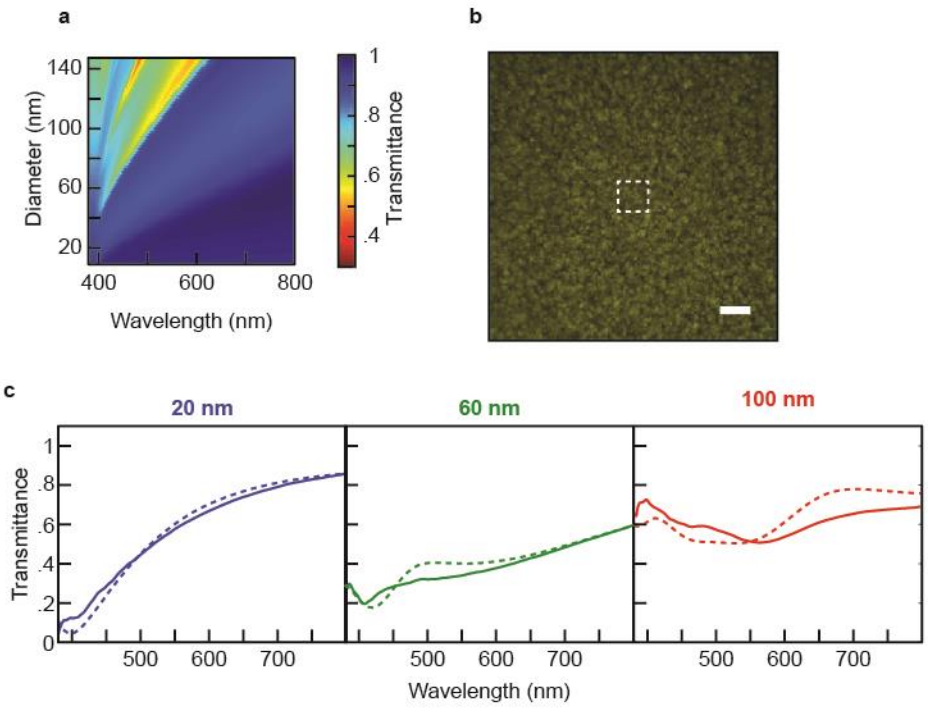


Figure 6.5| Measured and Simulated Transmittance. (a) Heatmap of simulated transmittance for single NWs of different diameters, diameter interval was 2 nm. (b) Example of the 50 μm^2 aperture used to measure transmittance on a section of a 60 nm network in PDMS; scale bar, 50 μm. (c) Simulated (dashed) and experimental transmittance data (solid) for 20 60 and 100 nm NWs. Simulated transmittance was plotted using a weighted average found using the magnitude of the Weibull distribution at each diameter.

used previously to describe the large color variance across different diameter NW samples as shown in Fig 6.3a. Additionally, when semiconductor NWs are exposed to a perpendicular electric field, 'leaky mode resonances' are formed, where resonant modes exist but the electric field is only semi-confined within the structure[19]. Similar to other resonant cavities, varying the diameter can shift the resonant frequency within the electromagnetic spectrum. We modeled this behavior using finite element analysis in COMSOL Multiphysics. The resulting simulated single NW diameter dependent transmittance is shown in Fig 6.5a. Simulated results were weighted based upon diameter data shown in Fig 6.6 and were compared to experimental transmittance values collected with a halogen lamp source from 380-700 nm as shown in Fig 6.5c. Simulated data was normalized to match the range of the experimental optical response. While magnitudes

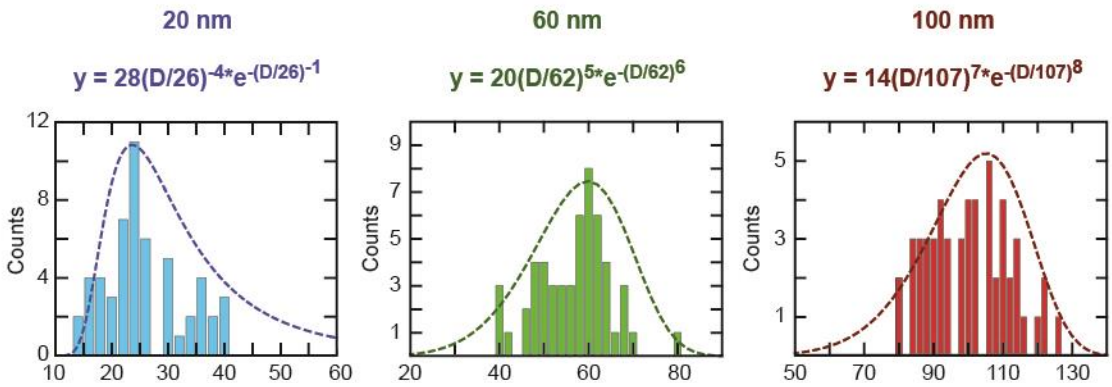


Figure 6.6| Grown NW Diameter Distribution. Histograms and Weibull fits demonstrating the diameter variation for NWs grown with 20, 60 and 100 nm gold catalysts. Diameters were measured from 100 distinct NWs for each diameter size and placed into 2 nm bins for each histogram. Qualitative Weibull distribution equations are listed above each histogram with maxima at 24, 60 and 105 nm for 20, 60 and 100 nm catalysts, respectively.

are dependent on the differing density between each diameter (which varies by about 3 orders of magnitude from 20 to 100 nm), the simulated diameter dependent optical response matches with the experimental result.

The electrical transport characteristics of the centimeter-scale NW networks were measured before and after lift-off from the growth substrate. Networks were constructed of 50 nm diameter n-type NWs with an encoded doping level of 2.5×10^{20} cm^{-3}, and they were grown on both Si/SiO_2 substrates and, for lift off, Si/SiO_2/Ge substrates. Macroscopic electrodes were fabricated on both films (Fig. 6.4a), and the substrate-free NW-PDMS film shows only a slight increase in resistance compared to networks on the substrate, as shown by the transport measurements in Fig. 4b. Moreover, the *I-V* curves of the films are linear over a broad voltage range (inset of Fig. 3b), demonstrating the high-quality of the Ohmic connections between the NWs. The approximate sheet resistance values of the two networks are 178 ± 11 and 164 ± 31 kΩ/square for the on-substrate and substrate-free films, respectively, showing no significant difference because of the lift-off process. A slight contact resistance is introduced from the PDMS, likely due to the decreased contact area between metal and encased NW. The performance of NW-PDMS films under strain was also probed by bending the films (inset of Fig.

6.4c). *I-V* data (Fig. 6.4c) shows a small, less than two-fold increase in resistance when measured across a 6 mm channel, demonstrating the mechanical robustness of the electrical conductivity

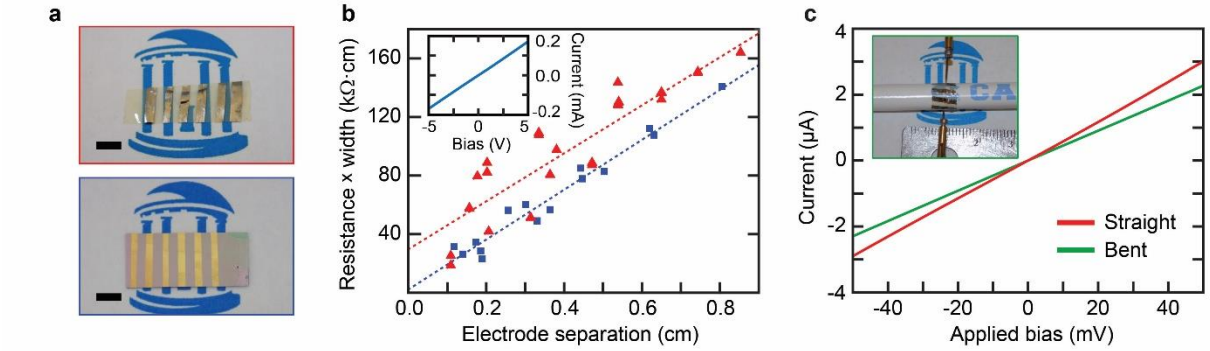


Figure 6.7| Macroscopic Network Electrical Measurements. (a) Photographs of PDMS embedded network (top) and network on growth substrate (bottom) with deposited electrodes for *I-V* measurements; scale bars, 5 mm. (b) Resistance multiplied by channel width as a function of electrode separation (*i.e.* channel length) for ~50 nm diameter NW networks measured on the Si growth substrate (blue squares) and on the substrate-free NW-PDMS film (red triangles). Dashed lines represent linear fits to the data, and the vertical offset of the dashed red line reflects a contact resistance of 39 ± 17 kΩ for the NW-PDMS film. Inset: *I-V* curve measured on the Si growth substrate for an electrode separation of 1.5 mm. (c) *I-V* data for the NW-PDMS film when in a straight (red) and bent (green) conformation with a radius of curvature of ~4 mm. Inset: photograph of the bent film contacted by electrical probe tips.

through the network. This behavior is consistent with flexibility observed in Ag NW networks[163] placed on polymer substrates.

While macroscopic electrical characterization is useful for determining the overall success of the welding process it cannot fully describe the electrical connectivity throughout the entire film. Conductive NW networks are commonly characterized by the percolation process, which states that networks of conducting sticks will not conduct between two electrodes until a critical density is reached. While we know from I-V data that 50 nm Si NWs will conduct across ~2 mm channels the number of percolation pathways and overall connectivity in the film is uncertain. To expound upon the electrical connectivity and percolation pathways in the NW network, voltage contrast imaging was employed. Voltage contrast is an inherent phenomenon that occurs when using electron microscopy on samples of dissimilar resistance while under an

electron or ion beam. It operates on the principle that different degrees of surface charging in a structure will lighten/darken the resulting SEM image since charging influences the number of electrons which can reach the detector. This natural contrast occurs when comparing floating and ground structures in the SEM[164] and in the past has been used to find faults in integrated circuits[165]. However, the same process has successfully been expanded to imaging the percolation threshold for metal NW networks undergoing electroformation[166]. Figure 6.5a-c shows the results for a large scale 100 nm diameter NW network grown on a thermal SiO_2/Si chip with a deposited metal electrode, which was used to connect the network to the SEM ground and apply bias. The entire NW network appears bright (Fig 6.5a) in contrast to the dark substrate when imaged with the ion beam, indicating that the positive charging resulting from the ion beam can dissipate throughout the entire network (and to the SEM ground) while positive charges gather on the surface of the floating substrate. To further demonstrate this contrast a small box was milled from the network, disconnecting the NWs within, as the contrast between 6.5b and 6.5c shows clearly. The electrically disconnected NWs within the box in 6.5c appear dark since the positive charges can no longer dissipate through the network to the SEM/FIB ground causing the network to darken like the substrate.

To determine whether the electrical connectivity is still present in small scale and compare with the large percolating films, 50 μm^2 NW networks were grown. Electrodes were contacted to three sides of the network, in two dense regions and one sparse, as well as one electrode which was completely disconnected to serve as a floating reference during voltage contrast. Electrical resistance measurements were taken using each combination of connected electrodes and compared to the AVC result shown in Fig 6.3f. The brighter and higher density section of the network (1-2) have lower resistance than the darker sections (2-3, 1-3) as shown in

the I-V results in Fig 6.3d. The I-V results show an order of magnitude decrease in current between the high density network electrodes (1-2) and the lower density areas of the network (2-3,1-3), which have resistances of 848 MΩ, 4200 MΩ and 4410 MΩ, respectively. This density dependence has been modeled in the past for percolating stick systems using Eq 6-3, which shows that conductivity increases quickly as NW density exceeds the critical percolation density[167].

$$\boldsymbol{\sigma \propto (N_{NW} - N_C)^t} \qquad \textbf{6-3}$$

Where σ is the conductivity, t is the scaling exponent and N_{NW} and N_C are the NW density and the percolation threshold density, respectively. Percolation paths often have lower resistances for higher density regions as the effective path length can be significantly shorter[168] and more conductivity pathways will form at higher densities. Conductivity within percolation networks will undergo order of magnitude changes due to increases in NW density between electrodes since the overall cross-sectional area of conducting elements is increased as well as the number of parallel conduction paths[122]. However, without knowing the exact junction resistance of each connection we cannot determine if the increase in resistance between 1-3 and 2-3 is due to parallel pathways, junction resistance, or contact resistance at electrode 3.

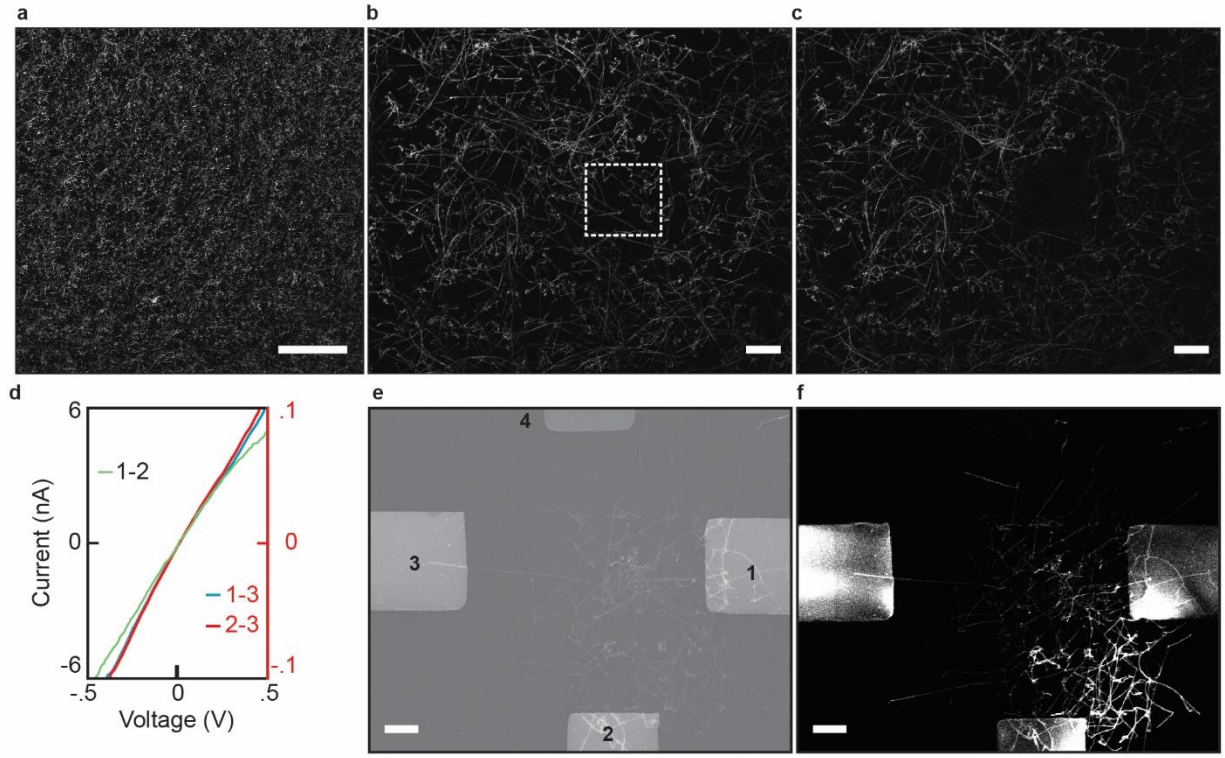


Figure 6.8| Visualizing Connectivity through AVC. Contrast image (a) taken using a Ga liquid metal ion source and an applied bias of -20 V between a 100 nm network and ground; scale bar, 100 μm. A small box (b) was cut around part of the network to demonstrate the contrast (c) between electrically connected and disconnected sections; scale bars, 10 μm. (d) I-V measurements for network paths between electrodes 1-3. 1-3,and 2-3 are plotted with the red current scale and 1-2 is plotted with the black. SEM images showing both the (e) entire network and (f) voltage contrast at -20 V; scale bars, 10 μm.

6.4 Conclusion

We have demonstrated a process for generating percolating networks of Si NWs which exhibit minimal change in resistance during lift off and after physical deformation. Networks can be placed on a variety of arbitrary substrates with minimal damage, opening the possibility for a wide variety of applications in optics and electronics. Additionally, voltage contrast confirmed the uniformity of the welding process since no disconnected regions were located across several growth substrates indicating a uniform anneal process. However, when taken down to a smaller

scale it was noted that the Si NW network may have higher junction resistances at certain regions, which could be due to distance from vacuum during the collapse process or orientation and resulting grain boundary of the NW junction.

Overall the results indicate that large scale ohmic Si NW networks can be generated with a result analogous to current metallic NW network. Additionally, with ordered growth and doping, semiconductor NW networks could be used for a variety of applications such as flexible/wearable electronics with potential biological, photovoltaic and energy storage applications.

CHAPTER 7: DECREASING THE THRESHOLD FOR SURFACE SELF DIFFUSION

7.1 Introduction

We previously reported nanoscale welding using a surface induced capillary diffusion process that commonly occurred at ~60% of the bulk melting temperature. While this process is viable for most CVD systems, industrial processes at temperatures above 500 °C are undesirable, since most industrial applications require low enough temperatures to not interfere with polymer/plastic processes. Additionally, for many semiconductor materials with high melting points such as Silicon Carbide (SiC) (MP: 2830 °C), reaching a sufficiently high temperature for surface diffusion is not viable through conventional means. To expand our process to more materials and increase relevance to industrial applications we attempted to lower the required temperature by increasing the local surface energy through several additional methods. We employed surface bombardment by high energy ions from a plasma and increased tribological force from added vibrational components.

Plasma enhanced CVD (PECVD) is commonly used to avoid high process temperatures, Si NWs have been grown at temperatures as low as 300 °C[169]. Instead of thermal degradation of the sample a plasma is employed to create a charged gas of the precursor species, which is then deposited on the substrate using the plasma kinetic energy. The plasma can be a mix of several gases, often the plasma consists of both the precursor gas and a carrier gas like Ar or H_2. Theoretically, using this process on already grown NWs would increase surface energy due to gas ions collisions with the surface.

7.2 Methods

Friction aided welding was attempted by first growing NWs and collapsing according to the previously reported process in Section 4.2 with a modified CVD set-up. Increased agitation was added using vibrating components (Digikey 28822-ND Vibration Motor Capsule) which were attached at either end of the quartz tube prior to growth. Once the sample was reinserted into the center of the quartz tube agitation was commenced and the sample underwent the same welding process (reported in Sec 4.2) at varying temperatures.

Plasma enhanced welding was accomplished using a home built RF-matching network which allowed plasma striking of 10 sccm H_2 and Ar gas at powers between 10-100W and at total pressures ~2 Torr. After the growth and collapse process NW samples were exposed to plasma of varying types and distances from the plasma. Plasma was generated by two copper bands around the quartz tube and placed upstream of the furnace.

7.3 Results

Tribological effects showed no significant impact on the surface diffusion process. We confirmed this by introducing large amounts of vibration at various anneal temperatures. At 850 °C 80 nm diameter NW showed no change in the weld quality and no increased surface instability at regions away from the weld. Reducing the ideal temperature by 10 °C and adding vibration did not weld 30 nm diameter NWs. It is likely that the macroscopic vibrational effect did not translate to the nanoscale system or the random orientation of NWs mitigated/dispersed the vibrational effect. This result is not surprising, considering that joining methods such as stir welding, cold welding and wafer bonding require extremely smooth and clean surfaces in addition to proper nanostructure orientation.

While frictional effects showed no change from the standard annealing process, plasma showed a strong influence on the welding process and the surface structure of the NWs. Figure 7.1 shows the SEM results and plasma positions for 600 °C anneal processes aided by both Ar and H_2 plasma. We believed Ar would be the ideal choice for increasing the surface energy of the NWs without causing etching due to its inert properties. However, Fig 7.1a shows that even when the Ar plasma fully encompassed the network at 800 °C there was no change to the surface or inter-NW junction formation. Even when temperature was increased to 840 °C, which is only 20 °C less than the ideal welding temperature, no effect was observed.

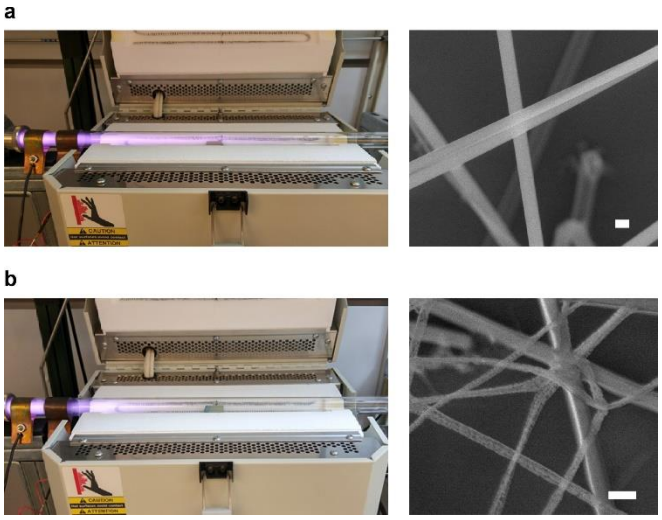


Figure 7.1| Plasma Welding of NWs. (a) Picture of Ar Plasma and SEM image of NWs afterwards. (b) Picture of H_2 plasma and SEM image of resulting NWs. Scale bars, 100 nm.

Unlike Ar, H_2 plasma (Fig 7.1b) had an etching effect on the NW surface. When plasma fully encompassed the entire network full etching of the NWs would occur within ~2 minutes. To negate this, we manipulated the plasma into a position further upstream, to avoid direct contact with the sample itself. Even with less power the H_2 plasma caused surface pitting and etching, as

shown by the SEM image in Fig 7.1b. The process is likely caused by atom abstraction of the hydrogen terminated silicon on the surface of the NW. When the reactive hydrogen ion reaches the surface, it will bond to the silicon causing a SiH_4 species to desorb from the surface. The open bonds to the surrounding Si will then be filled by other hydrogen plasma atoms causing the desorption process to repeat.

7.4 Conclusion

Several methods were tested to decrease the required anneal temperature for the NW welding process. Plasma assisted and tribological methods were attempted to decrease the anneal temperature by adding to the surface energy. Tribological factors were shown to have no effect on the welding temperature or quality of the weld, likely due to the minimal frictional energy generated at contact points between NWs. Plasma assisted annealing also did not show any beneficial effect on the welding process. H_2 plasma acted as a surface etchant on the NWs, most likely resulting from the formation of SiH_x leaving groups. When Ar plasma was introduced no additional change was found in the overall welding process or the temperature at which the process occurred. While plasma assisted welding may be useful in the future it requires more study and may require an additional additive process, similar to the use of a PECVD, to decrease the process temperature.

CHAPTER 8: CONCLUSIONS AND FUTURE WORK

8.1 NW Weld Methodology and Characterization

We determined that additive methods for weld formation were not necessary when proper precautions were taken to ensure a native oxide free NW surface. Liquid nitrogen was determined to be the best for collapse since the solvent needed to be oxygen free and non-reactive with the hydrogen terminated Si NW surface. In general other oxygen free solvents such as hexanes and chloroform may also be used for collapse, and some chlorine containing solvents may provide an improved result since previous reports have shown Cl terminated Si NWs. We have run preliminary tests on Si NWs grown with Cl terminated surfaces and found little change in weld temperature and quality. In addition, testing new solvents may open pathways for welding mechanically transferred or otherwise ordered NWs as BHF etching with oxygen free rinse solvents could possibly allow for welding arrays that had already formed native oxide. NW welds were shown through EDS and HR-TEM to be free of native oxide in addition to being single crystalline with the exception of a single grain boundary that differed depending on the orientation at the point of contact. The added junction resistance of ~70 kΩ matched well with previous R_j/ρ for metallic NWs. The effect of contact angle on both junction resistance and crystallinity are interesting areas for future exploration. Similar research on aligned InAs NWs indicates that alignment will have a significant impact, with NWs at proper contact angles yielding single crystalline, 0 Ω junctions. Diameter and weld temperature were determined for Si NWs, though more research could improve the accuracy of the transitions between the 3 zones

(No change, surface diffusion, and surface instability). With enough data, a mathematical model could be developed in order to more accurately predict welding temperature from empirical data. Coupled with simulations mentioned below, the ideal weld conditions for any nanomaterial could be predicted.

8.2 Modeling Capillarity Induced Surface Diffusion between Nanostructures

Models were developed for two separate aspects of NW welding. Surface Evolver was used to simulate the change in geometry for contacted NWs until a minimum surface energy was reached. Surface evolver does have functionality that allows for surface energy minimization based on crystallinity in addition to surface tension, which may open pathways for modeling of faceted crystalline nanostructures and predicting geometry changes for different crystalline faces. Using the methodology explained within this work, different initial geometries such as nanotubes, nanospheres and nanorods with non-circular cross sections can be modeled and weld morphologies can be predicted. COMSOL finite element analysis supported the conclusion of a capillarity driven surface diffusion mechanism for weld formation and accurately predicted several qualitative differences in weld/instability morphology between parallel and perpendicular NWs. In addition to qualitative predictions about geometries, we believe that the simulations can provide insight into determining experimental temperatures for surface diffusion in other semiconductor or even metallic/insulating materials.

8.3 Macroscopic NW Networks

Arrays consisting of millions of interconnected NWs were generated with varying density, NW diameter and collapse height. We demonstrated a Ge underetch/PDMS spin process to then embed these networks within transparent PDMS stamps. The resulting film was highly

transparent and mechanically robust. In addition, experimental optical response tracked well with simulated results for frequency dependent resonance shifts in single NWs. In addition to high transparency NWs were found to have relatively uniform electrical connectivity, which was confirmed using AVC. The small >2x increase in resistance when the NW/PDMS film underwent mechanical strain showed that the resulting PDMS films were robust enough for integration into flexible electronics, though repeated stretch/strain tests would be required to determine the extent of that viability. However, the connectivity, mechanical robustness, and transparency are all factors to consider when imagining future device applications. Applications such as tinted PV windows, wearable tribological/PV energy generators, and biological detectors are technological avenues that warrant investigation.

APPENDIX A: COMMANDS USED IN SURFACE EVOLVER

U - Toggle Conjugate Gradient Method

g – Iterate

r - Refine trainagulation

l - Subdivide long edges

V - Vertex averaging

u – Equiangulate

w – weed out small faces

s – Display

Typical Evolution Process:

Step	Command	Input/Note
1	U	
2	r	
3	l	.05
4	r	
5	r	
6	V	
7	u	Repeat 6/7 for random mesh
8	g	
9	w	1E-3
10	V	
11	u	Repeat 8-11 until desired surface

APPENDIX B: SURFACE EVOLVER CODE FOR WELDED NW GEOMETRY

Equivalent Perpendicular NWs

```
//Radius of cylinder

PARAMETER radius = 1

vertices

//circle 1 vertices

1 radius*cos(0 + pi/20) 1-cos(pi/20)+radius*sin(0 + pi/20) -20
2 radius*cos(pi/10 + pi/20) 1-cos(pi/20)+radius*sin(pi/10 + pi/20) -20
3 radius*cos(2*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(2*pi/10 + pi/20) -20
4 radius*cos(3*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(3*pi/10 + pi/20) -20
5 radius*cos(4*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(4*pi/10 + pi/20) -20
6 radius*cos(5*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(5*pi/10 + pi/20) -20
7 radius*cos(6*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(6*pi/10 + pi/20) -20
8 radius*cos(7*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(7*pi/10 + pi/20) -20
9 radius*cos(8*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(8*pi/10 + pi/20) -20
10 radius*cos(9*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(9*pi/10 + pi/20) -20
11 radius*cos(10*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(10*pi/10 + pi/20) -20
12 radius*cos(11*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(11*pi/10 + pi/20) -20
13 radius*cos(12*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(12*pi/10 + pi/20) -20
14 radius*cos(13*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(13*pi/10 + pi/20) -20
15 radius*cos(14*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(14*pi/10 + pi/20) -20
16 radius*cos(15*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(15*pi/10 + pi/20) -20
17 radius*cos(16*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(16*pi/10 + pi/20) -20
18 radius*cos(17*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(17*pi/10 + pi/20) -20
19 radius*cos(18*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(18*pi/10 + pi/20) -20
20 radius*cos(19*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(19*pi/10 + pi/20) -20


//circle 2 vertices

41 radius*cos(0 + pi/20) 1-cos(pi/20)+radius*sin(0 + pi/20) 30
42 radius*cos(pi/10 + pi/20) 1-cos(pi/20)+radius*sin(pi/10 + pi/20) 30
43 radius*cos(2*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(2*pi/10 + pi/20) 30
44 radius*cos(3*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(3*pi/10 + pi/20) 30
45 radius*cos(4*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(4*pi/10 + pi/20) 30
46 radius*cos(5*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(5*pi/10 + pi/20) 30
47 radius*cos(6*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(6*pi/10 + pi/20) 30
48 radius*cos(7*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(7*pi/10 + pi/20) 30
49 radius*cos(8*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(8*pi/10 + pi/20) 30
50 radius*cos(9*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(9*pi/10 + pi/20) 30
51 radius*cos(10*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(10*pi/10 + pi/20) 30
52 radius*cos(11*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(11*pi/10 + pi/20) 30
53 radius*cos(12*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(12*pi/10 + pi/20) 30
54 radius*cos(13*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(13*pi/10 + pi/20) 30
55 radius*cos(14*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(14*pi/10 + pi/20) 30
56 radius*cos(15*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(15*pi/10 + pi/20) 30
57 radius*cos(16*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(16*pi/10 + pi/20) 30
58 radius*cos(17*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(17*pi/10 + pi/20) 30
```

59 radius*cos(18*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(18*pi/10 + pi/20) 30
60 radius*cos(19*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(19*pi/10 + pi/20) 30

//circle 3 vertices

1001 25 1+cos(pi/20)+radius*cos(0 + pi/20) 5+radius*sin(0 + pi/20)
1002 25 1+cos(pi/20)+radius*cos(pi/10 + pi/20) 5+radius*sin(pi/10 + pi/20)
1003 25 1+cos(pi/20)+radius*cos(2*pi/10 + pi/20) 5+radius*sin(2*pi/10 + pi/20)
1004 25 1+cos(pi/20)+radius*cos(3*pi/10 + pi/20) 5+radius*sin(3*pi/10 + pi/20)
1005 25 1+cos(pi/20)+radius*cos(4*pi/10 + pi/20) 5+radius*sin(4*pi/10 + pi/20)
1006 25 1+cos(pi/20)+radius*cos(5*pi/10 + pi/20) 5+radius*sin(5*pi/10 + pi/20)
1007 25 1+cos(pi/20)+radius*cos(6*pi/10 + pi/20) 5+radius*sin(6*pi/10 + pi/20)
1008 25 1+cos(pi/20)+radius*cos(7*pi/10 + pi/20) 5+radius*sin(7*pi/10 + pi/20)
1009 25 1+cos(pi/20)+radius*cos(8*pi/10 + pi/20) 5+radius*sin(8*pi/10 + pi/20)
1010 25 1+cos(pi/20)+radius*cos(9*pi/10 + pi/20) 5+radius*sin(9*pi/10 + pi/20)
1011 25 1+cos(pi/20)+radius*cos(10*pi/10 + pi/20) 5+radius*sin(10*pi/10 + pi/20)
1012 25 1+cos(pi/20)+radius*cos(11*pi/10 + pi/20) 5+radius*sin(11*pi/10 + pi/20)
1013 25 1+cos(pi/20)+radius*cos(12*pi/10 + pi/20) 5+radius*sin(12*pi/10 + pi/20)
1014 25 1+cos(pi/20)+radius*cos(13*pi/10 + pi/20) 5+radius*sin(13*pi/10 + pi/20)
1015 25 1+cos(pi/20)+radius*cos(14*pi/10 + pi/20) 5+radius*sin(14*pi/10 + pi/20)
1016 25 1+cos(pi/20)+radius*cos(15*pi/10 + pi/20) 5+radius*sin(15*pi/10 + pi/20)
1017 25 1+cos(pi/20)+radius*cos(16*pi/10 + pi/20) 5+radius*sin(16*pi/10 + pi/20)
1018 25 1+cos(pi/20)+radius*cos(17*pi/10 + pi/20) 5+radius*sin(17*pi/10 + pi/20)
1019 25 1+cos(pi/20)+radius*cos(18*pi/10 + pi/20) 5+radius*sin(18*pi/10 + pi/20)
1020 25 1+cos(pi/20)+radius*cos(19*pi/10 + pi/20) 5+radius*sin(19*pi/10 + pi/20)

//circle 4 vertices

1041 -25 1+cos(pi/20)+radius*cos(0 + pi/20) 5+radius*sin(0 + pi/20)
1042 -25 1+cos(pi/20)+radius*cos(pi/10 + pi/20) 5+radius*sin(pi/10 + pi/20)
1043 -25 1+cos(pi/20)+radius*cos(2*pi/10 + pi/20) 5+radius*sin(2*pi/10 + pi/20)
1044 -25 1+cos(pi/20)+radius*cos(3*pi/10 + pi/20) 5+radius*sin(3*pi/10 + pi/20)
1045 -25 1+cos(pi/20)+radius*cos(4*pi/10 + pi/20) 5+radius*sin(4*pi/10 + pi/20)
1046 -25 1+cos(pi/20)+radius*cos(5*pi/10 + pi/20) 5+radius*sin(5*pi/10 + pi/20)
1047 -25 1+cos(pi/20)+radius*cos(6*pi/10 + pi/20) 5+radius*sin(6*pi/10 + pi/20)
1048 -25 1+cos(pi/20)+radius*cos(7*pi/10 + pi/20) 5+radius*sin(7*pi/10 + pi/20)
1049 -25 1+cos(pi/20)+radius*cos(8*pi/10 + pi/20) 5+radius*sin(8*pi/10 + pi/20)
1050 -25 1+cos(pi/20)+radius*cos(9*pi/10 + pi/20) 5+radius*sin(9*pi/10 + pi/20)
1051 -25 1+cos(pi/20)+radius*cos(10*pi/10 + pi/20) 5+radius*sin(10*pi/10 + pi/20)
1052 -25 1+cos(pi/20)+radius*cos(11*pi/10 + pi/20) 5+radius*sin(11*pi/10 + pi/20)
1053 -25 1+cos(pi/20)+radius*cos(12*pi/10 + pi/20) 5+radius*sin(12*pi/10 + pi/20)
1054 -25 1+cos(pi/20)+radius*cos(13*pi/10 + pi/20) 5+radius*sin(13*pi/10 + pi/20)
1055 -25 1+cos(pi/20)+radius*cos(14*pi/10 + pi/20) 5+radius*sin(14*pi/10 + pi/20)
1056 -25 1+cos(pi/20)+radius*cos(15*pi/10 + pi/20) 5+radius*sin(15*pi/10 + pi/20)
1057 -25 1+cos(pi/20)+radius*cos(16*pi/10 + pi/20) 5+radius*sin(16*pi/10 + pi/20)
1058 -25 1+cos(pi/20)+radius*cos(17*pi/10 + pi/20) 5+radius*sin(17*pi/10 + pi/20)
1059 -25 1+cos(pi/20)+radius*cos(18*pi/10 + pi/20) 5+radius*sin(18*pi/10 + pi/20)
1060 -25 1+cos(pi/20)+radius*cos(19*pi/10 + pi/20) 5+radius*sin(19*pi/10 + pi/20)

//end centers

81 0 0 -22

82 0 0 32
1081 27 2 5
1082 -27 2 5

//connection points
83 radius*cos(4*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(4*pi/10 + pi/20) 5-sin(pi/20)
84 radius*cos(5*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(5*pi/10 + pi/20) 5-sin(pi/20)
85 radius*cos(4*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(4*pi/10 + pi/20) 5+sin(pi/20)
86 radius*cos(5*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(5*pi/10 + pi/20) 5+sin(pi/20)

edges

//circle 1 edges

1 1 2
2 2 3
3 3 4
4 4 5
5 5 6
6 6 7
7 7 8
8 8 9
9 9 10
10 10 11
11 11 12
12 12 13
13 13 14
14 14 15
15 15 16
16 16 17
17 17 18
18 18 19
19 19 20
20 20 1

//circle 2 edges

41 41 42
42 42 43
43 43 44
44 44 45
45 45 46
46 46 47
47 47 48
48 48 49
49 49 50
50 50 51
51 51 52
52 52 53
53 53 54
54 54 55
55 55 56
56 56 57
57 57 58
58 58 59

59 59 60
60 60 41

//circle 3 edges

1001 1001 1002
1002 1002 1003
1003 1003 1004
1004 1004 1005
1005 1005 1006
1006 1006 1007
1007 1007 1008
1008 1008 1009
1009 1009 1010
1010 1010 1011
1011 1011 1012
1012 1012 1013
1013 1013 1014
1014 1014 1015
1015 1015 1016
1016 1016 1017
1017 1017 1018
1018 1018 1019
1019 1019 1020
1020 1020 1001

//circle 4 edges

1041 1041 1042
1042 1042 1043
1043 1043 1044
1044 1044 1045
1045 1045 1046
1046 1046 1047
1047 1047 1048
1048 1048 1049
1049 1049 1050
1050 1050 1051
1051 1051 1052
1052 1052 1053
1053 1053 1054
1054 1054 1055
1055 1055 1056
1056 1056 1057
1057 1057 1058
1058 1058 1059
1059 1059 1060
1060 1060 1041

//connect circle 1 to circle 2

81 1 41
82 2 42
83 3 43

84 4 44
87 7 47
88 8 48
89 9 49
90 10 50
91 11 51
92 12 52
93 13 53
94 14 54
95 15 55
96 16 56
97 17 57
98 18 58
99 19 59
100 20 60

//connect circle 3 to circle 4

1081 1001 1041
1082 1002 1042
1083 1003 1043
1084 1004 1044
1085 1005 1045
1086 1006 1046
1087 1007 1047
1088 1008 1048
1089 1009 1049
1092 1012 1052
1093 1013 1053
1094 1014 1054
1095 1015 1055
1096 1016 1056
1097 1017 1057
1098 1018 1058
1099 1019 1059
1100 1020 1060

//Circle 1 connect to center

121 81 1
122 81 2
123 81 3
124 81 4
125 81 5
126 81 6
127 81 7
128 81 8
129 81 9
130 81 10
131 81 11
132 81 12
133 81 13
134 81 14
135 81 15

136 81 16
137 81 17
138 81 18
139 81 19
140 81 20

//Circle 2 connect to center

161 82 41
162 82 42
163 82 43
164 82 44
165 82 45
166 82 46
167 82 47
168 82 48
169 82 49
170 82 50
171 82 51
172 82 52
173 82 53
174 82 54
175 82 55
176 82 56
177 82 57
178 82 58
179 82 59
180 82 60

//Circle 3 connect to center

1121 1081 1001
1122 1081 1002
1123 1081 1003
1124 1081 1004
1125 1081 1005
1126 1081 1006
1127 1081 1007
1128 1081 1008
1129 1081 1009
1130 1081 1010
1131 1081 1011
1132 1081 1012
1133 1081 1013
1134 1081 1014
1135 1081 1015
1136 1081 1016
1137 1081 1017
1138 1081 1018
1139 1081 1019
1140 1081 1020

//Circle 4 connect to center

1161 1082 1041
1162 1082 1042
1163 1082 1043
1164 1082 1044
1165 1082 1045
1166 1082 1046
1167 1082 1047
1168 1082 1048
1169 1082 1049
1170 1082 1050
1171 1082 1051
1172 1082 1052
1173 1082 1053
1174 1082 1054
1175 1082 1055
1176 1082 1056
1177 1082 1057
1178 1082 1058
1179 1082 1059
1180 1082 1060

//Connect circle 1 to center
200 5 83
201 6 84

//Connect circle 2 to center
202 45 85
203 46 86

//Connect circle 3 to center
204 1010 85
205 1011 83

//Connect circle 4 to center
206 1050 86
207 1051 84

//Center square
208 83 85
209 85 86
210 86 84
211 84 83

faces

//Cyl 1 side faces

1 1 82 -41 -81
2 2 83 -42 -82
3 3 84 -43 -83
7 7 88 -47 -87
8 8 89 -48 -88
9 9 90 -49 -89
10 10 91 -50 -90

11 11 92 -51 -91
12 12 93 -52 -92
13 13 94 -53 -93
14 14 95 -54 -94
15 15 96 -55 -95
16 16 97 -56 -96
17 17 98 -57 -97
18 18 99 -58 -98
19 19 100 -59 -99
20 20 81 -60 -100

//Faces involving midpoints

21 5 201 211 -200
22 202 209 -203 -45
23 204 -208 -205 -1010
24 1050 207 -210 -206
25 6 87 -46 203 210 -201
26 4 200 208 -202 -44 -84
27 205 -211 -207 1051 -1092 -1011
28 1089 1049 206 -209 -204 -1009
//29 208 209 210 211

//Cyl2 side faces

1001 1081 1041 -1082 -1001
1002 1082 1042 -1083 -1002
1003 1083 1043 -1084 -1003
1004 1084 1044 -1085 -1004
1005 1085 1045 -1086 -1005
1006 1086 1046 -1087 -1006
1007 1087 1047 -1088 -1007
1008 1088 1048 -1089 -1008
1012 1092 1052 -1093 -1012
1013 1093 1053 -1094 -1013
1014 1094 1054 -1095 -1014
1015 1095 1055 -1096 -1015
1016 1096 1056 -1097 -1016
1017 1097 1057 -1098 -1017
1018 1098 1058 -1099 -1018
1019 1099 1059 -1100 -1019
1020 1100 1060 -1081 -1020

//circle 1 end faces

41 -121 122 -1
42 -122 123 -2
43 -123 124 -3
44 -124 125 -4
45 -125 126 -5
46 -126 127 -6
47 -127 128 -7
48 -128 129 -8
49 -129 130 -9
50 -130 131 -10

51 -131 132 -11
52 -132 133 -12
53 -133 134 -13
54 -134 135 -14
55 -135 136 -15
56 -136 137 -16
57 -137 138 -17
58 -138 139 -18
59 -139 140 -19
60 -140 121 -20

//circle 2 end faces

81 41 -162 161
82 42 -163 162
83 43 -164 163
84 44 -165 164
85 45 -166 165
86 46 -167 166
87 47 -168 167
88 48 -169 168
89 49 -170 169
90 50 -171 170
91 51 -172 171
92 52 -173 172
93 53 -174 173
94 54 -175 174
95 55 -176 175
96 56 -177 176
97 57 -178 177
98 58 -179 178
99 59 -180 179
100 60 -161 180

//circle 3 end faces

1041 1001 -1122 1121
1042 1002 -1123 1122
1043 1003 -1124 1123
1044 1004 -1125 1124
1045 1005 -1126 1125
1046 1006 -1127 1126
1047 1007 -1128 1127
1048 1008 -1129 1128
1049 1009 -1130 1129
1050 1010 -1131 1130
1051 1011 -1132 1131
1052 1012 -1133 1132
1053 1013 -1134 1133
1054 1014 -1135 1134
1055 1015 -1136 1135
1056 1016 -1137 1136
1057 1017 -1138 1137
1058 1018 -1139 1138

1059 1019 -1140 1139
1060 1020 -1121 1140

//circle 4 end faces

1081 -1161 1162 -1041
1082 -1162 1163 -1042
1083 -1163 1164 -1043
1084 -1164 1165 -1044
1085 -1165 1166 -1045
1086 -1166 1167 -1046
1087 -1167 1168 -1047
1088 -1168 1169 -1048
1089 -1169 1170 -1049
1090 -1170 1171 -1050
1091 -1171 1172 -1051
1092 -1172 1173 -1052
1093 -1173 1174 -1053
1094 -1174 1175 -1054
1095 -1175 1176 -1055
1096 -1176 1177 -1056
1097 -1177 1178 -1057
1098 -1178 1179 -1058
1099 -1179 1180 -1059
1100 -1180 1161 -1060

bodies

1 1 2 3 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 25 26 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 23 24 27 28 1001 1002 1003 1004 1005 1006 1007 1008 1012 1013 1014 1015 1016 1017 1018 1019 1020 1041 1042 1043 1044 1045 1045 1046 1047 1048 1049 1050 1051 1052 1053 1054 1055 1056 1057 1058 1059 1060 1081 1082 1083 1084 1085 1086 1087 1088 1089 1090 1091 1092 1093 1094 1095 1096 1097 1098 1099 1100 volume 317.257447558279

Equivalent Parallel NWs

//Radius of cylinder for both

PARAMETER radius = 1

PARAMETER shift = cos(9*pi/180)*radius //Vertical Shift of the second cylinder

//Cylinder 1 Bottom

vertices

//circle 1 vertices

1 radius*cos(0 + pi/20) 1-cos(pi/20)+radius*sin(0 + pi/20) -25
2 radius*cos(pi/10 + pi/20) 1-cos(pi/20)+radius*sin(pi/10 + pi/20) -25
3 radius*cos(2*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(2*pi/10 + pi/20) -25

4 radius*cos(3*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(3*pi/10 + pi/20) -25
5 radius*cos(4*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(4*pi/10 + pi/20) -25
6 radius*cos(5*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(5*pi/10 + pi/20) -25
7 radius*cos(6*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(6*pi/10 + pi/20) -25
8 radius*cos(7*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(7*pi/10 + pi/20) -25
9 radius*cos(8*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(8*pi/10 + pi/20) -25
10 radius*cos(9*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(9*pi/10 + pi/20) -25
11 radius*cos(10*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(10*pi/10 + pi/20) -25
12 radius*cos(11*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(11*pi/10 + pi/20) -25
13 radius*cos(12*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(12*pi/10 + pi/20) -25
14 radius*cos(13*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(13*pi/10 + pi/20) -25
15 radius*cos(14*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(14*pi/10 + pi/20) -25
16 radius*cos(15*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(15*pi/10 + pi/20) -25
17 radius*cos(16*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(16*pi/10 + pi/20) -25
18 radius*cos(17*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(17*pi/10 + pi/20) -25
19 radius*cos(18*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(18*pi/10 + pi/20) -25
20 radius*cos(19*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(19*pi/10 + pi/20) -25

//circle 2 vertices

41 radius*cos(0 + pi/20) 1-cos(pi/20)+radius*sin(0 + pi/20) 25
42 radius*cos(pi/10 + pi/20) 1-cos(pi/20)+radius*sin(pi/10 + pi/20) 25
43 radius*cos(2*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(2*pi/10 + pi/20) 25
44 radius*cos(3*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(3*pi/10 + pi/20) 25
45 radius*cos(4*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(4*pi/10 + pi/20) 25
46 radius*cos(5*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(5*pi/10 + pi/20) 25
47 radius*cos(6*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(6*pi/10 + pi/20) 25
48 radius*cos(7*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(7*pi/10 + pi/20) 25
49 radius*cos(8*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(8*pi/10 + pi/20) 25
50 radius*cos(9*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(9*pi/10 + pi/20) 25
51 radius*cos(10*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(10*pi/10 + pi/20) 25
52 radius*cos(11*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(11*pi/10 + pi/20) 25
53 radius*cos(12*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(12*pi/10 + pi/20) 25
54 radius*cos(13*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(13*pi/10 + pi/20) 25
55 radius*cos(14*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(14*pi/10 + pi/20) 25
56 radius*cos(15*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(15*pi/10 + pi/20) 25
57 radius*cos(16*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(16*pi/10 + pi/20) 25
58 radius*cos(17*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(17*pi/10 + pi/20) 25
59 radius*cos(18*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(18*pi/10 + pi/20) 25
60 radius*cos(19*pi/10 + pi/20) 1-cos(pi/20)+radius*sin(19*pi/10 + pi/20) 25

//Cylinder 2 Top

//circle 3 vertices

1001 radius*cos(0 + pi/20) shift+cos(pi/20)+radius*sin(0 + pi/20) -25
1002 radius*cos(pi/10 + pi/20) shift+cos(pi/20)+radius*sin(pi/10 + pi/20) -25
1003 radius*cos(2*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(2*pi/10 + pi/20) -25
1004 radius*cos(3*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(3*pi/10 + pi/20) -25
1005 radius*cos(4*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(4*pi/10 + pi/20) -25
1006 radius*cos(5*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(5*pi/10 + pi/20) -25
1007 radius*cos(6*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(6*pi/10 + pi/20) -25
1008 radius*cos(7*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(7*pi/10 + pi/20) -25
1009 radius*cos(8*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(8*pi/10 + pi/20) -25
1010 radius*cos(9*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(9*pi/10 + pi/20) -25

1011 radius*cos(10*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(10*pi/10 + pi/20) -25
1012 radius*cos(11*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(11*pi/10 + pi/20) -25
1013 radius*cos(12*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(12*pi/10 + pi/20) -25
1014 radius*cos(13*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(13*pi/10 + pi/20) -25
1017 radius*cos(16*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(16*pi/10 + pi/20) -25
1018 radius*cos(17*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(17*pi/10 + pi/20) -25
1019 radius*cos(18*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(18*pi/10 + pi/20) -25
1020 radius*cos(19*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(19*pi/10 + pi/20) -25

//circle 4 vertices

1041 radius*cos(0 + pi/20) shift+cos(pi/20)+radius*sin(0 + pi/20) 25
1042 radius*cos(pi/10 + pi/20) shift+cos(pi/20)+radius*sin(pi/10 + pi/20) 25
1043 radius*cos(2*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(2*pi/10 + pi/20) 25
1044 radius*cos(3*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(3*pi/10 + pi/20) 25
1045 radius*cos(4*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(4*pi/10 + pi/20) 25
1046 radius*cos(5*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(5*pi/10 + pi/20) 25
1047 radius*cos(6*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(6*pi/10 + pi/20) 25
1048 radius*cos(7*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(7*pi/10 + pi/20) 25
1049 radius*cos(8*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(8*pi/10 + pi/20) 25
1050 radius*cos(9*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(9*pi/10 + pi/20) 25
1051 radius*cos(10*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(10*pi/10 + pi/20) 25
1052 radius*cos(11*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(11*pi/10 + pi/20) 25
1053 radius*cos(12*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(12*pi/10 + pi/20) 25
1054 radius*cos(13*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(13*pi/10 + pi/20) 25
1057 radius*cos(16*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(16*pi/10 + pi/20) 25
1058 radius*cos(17*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(17*pi/10 + pi/20) 25
1059 radius*cos(18*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(18*pi/10 + pi/20) 25
1060 radius*cos(19*pi/10 + pi/20) shift+cos(pi/20)+radius*sin(19*pi/10 + pi/20) 25

//end centers

81 0 0 -27
82 0 0 27
1081 0 2*radius -27
1082 0 2*radius 27

edges

//circle 1 edges

1 1 2
2 2 3
3 3 4
4 4 5
5 5 6
6 6 7
7 7 8
8 8 9
9 9 10
10 10 11

11 11 12
12 12 13
13 13 14
14 14 15
15 15 16
16 16 17
17 17 18
18 18 19
19 19 20
20 20 1

//circle 2 edges

41 41 42
42 42 43
43 43 44
44 44 45
45 45 46
46 46 47
47 47 48
48 48 49
49 49 50
50 50 51
51 51 52
52 52 53
53 53 54
54 54 55
55 55 56
56 56 57
57 57 58
58 58 59
59 59 60
60 60 41

//circle 3 edges

1001 1001 1002
1002 1002 1003
1003 1003 1004
1004 1004 1005
1005 1005 1006
1006 1006 1007
1007 1007 1008
1008 1008 1009
1009 1009 1010
1010 1010 1011
1011 1011 1012
1012 1012 1013
1013 1013 1014
1014 1014 6
1016 5 1017
1017 1017 1018
1018 1018 1019
1019 1019 1020

1020 1020 1001

//circle 4 edges

1041 1041 1042
1042 1042 1043
1043 1043 1044
1044 1044 1045
1045 1045 1046
1046 1046 1047
1047 1047 1048
1048 1048 1049
1049 1049 1050
1050 1050 1051
1051 1051 1052
1052 1052 1053
1053 1053 1054
1054 1054 46
1056 45 1057
1057 1057 1058
1058 1058 1059
1059 1059 1060
1060 1060 1041

//Edges for open parallel face

85 5 45
86 6 46

//connect circle 1 to circle 2

81 1 41
82 2 42
83 3 43
84 4 44
87 7 47
88 8 48
89 9 49
90 10 50
91 11 51
92 12 52
93 13 53
94 14 54
95 15 55
96 16 56
97 17 57
98 18 58
99 19 59
100 20 60

//connect circle 3 to circle 4

1081 1001 1041
1082 1002 1042

1083 1003 1043
1084 1004 1044
1085 1005 1045
1086 1006 1046
1087 1007 1047
1088 1008 1048
1089 1009 1049
1090 1010 1050
1091 1011 1051
1092 1012 1052
1093 1013 1053
1094 1014 1054
1097 1017 1057
1098 1018 1058
1099 1019 1059
1100 1020 1060

//Circle 1 connect to center

121 81 1
122 81 2
123 81 3
124 81 4
125 81 5
126 81 6
127 81 7
128 81 8
129 81 9
130 81 10
131 81 11
132 81 12
133 81 13
134 81 14
135 81 15
136 81 16
137 81 17
138 81 18
139 81 19
140 81 20

//Circle 2 connect to center

161 82 41
162 82 42
163 82 43
164 82 44
165 82 45
166 82 46
167 82 47
168 82 48
169 82 49
170 82 50
171 82 51
172 82 52

173 82 53
174 82 54
175 82 55
176 82 56
177 82 57
178 82 58
179 82 59
180 82 60

//Circle 3 connect to center

1121 1081 1001
1122 1081 1002
1123 1081 1003
1124 1081 1004
1125 1081 1005
1126 1081 1006
1127 1081 1007
1128 1081 1008
1129 1081 1009
1130 1081 1010
1131 1081 1011
1132 1081 1012
1133 1081 1013
1134 1081 1014
1135 1081 5
1136 1081 6
1137 1081 1017
1138 1081 1018
1139 1081 1019
1140 1081 1020

//Circle 4 connect to center

1161 1082 1041
1162 1082 1042
1163 1082 1043
1164 1082 1044
1165 1082 1045
1166 1082 1046
1167 1082 1047
1168 1082 1048
1169 1082 1049
1170 1082 1050
1171 1082 1051
1172 1082 1052
1173 1082 1053
1174 1082 1054
1175 1082 45
1176 1082 46
1177 1082 1057
1178 1082 1058
1179 1082 1059

1180 1082 1060

faces

//Cyl 1 side faces, negative sign traverses vector in direction opposite to definition

1 1 82 -41 -81
2 2 83 -42 -82
3 3 84 -43 -83
4 4 85 -44 -84
6 6 87 -46 -86
7 7 88 -47 -87
8 8 89 -48 -88
9 9 90 -49 -89
10 10 91 -50 -90
11 11 92 -51 -91
12 12 93 -52 -92
13 13 94 -53 -93
14 14 95 -54 -94
15 15 96 -55 -95
16 16 97 -56 -96
17 17 98 -57 -97
18 18 99 -58 -98
19 19 100 -59 -99
20 20 81 -60 -100

//Cyl2 side faces

1001 1001 1082 -1041 -1081
1002 1002 1083 -1042 -1082
1003 1003 1084 -1043 -1083
1004 1004 1085 -1044 -1084
1005 1005 1086 -1045 -1085
1006 1006 1087 -1046 -1086
1007 1007 1088 -1047 -1087
1008 1008 1089 -1048 -1088
1009 1009 1090 -1049 -1089
1010 1010 1091 -1050 -1090
1011 1011 1092 -1051 -1091
1012 1012 1093 -1052 -1092
1013 1013 1094 -1053 -1093
1014 1014 86 -1054 -1094 // Border Face #Correct Geom
//1015 85 1055 -1055 -1095 //Removed face cyl 2
1016 1016 1097 -1056 -85 // Border Face #Correct Geom
1017 1017 1098 -1057 -1097   //Orig 1097 1057 -1098 -1017
1018 1018 1099 -1058 -1098
1019 1019 1100 -1059 -1099
1020 1020 1081 -1060 -1100   //Originally 1100 1060 -1081 -1020

//circle 1 end faces

41 -121 122 -1

42 -122 123 -2
43 -123 124 -3
44 -124 125 -4
45 -125 126 -5
46 -126 127 -6
47 -127 128 -7
48 -128 129 -8
49 -129 130 -9
50 -130 131 -10
51 -131 132 -11
52 -132 133 -12
53 -133 134 -13
54 -134 135 -14
55 -135 136 -15
56 -136 137 -16
57 -137 138 -17
58 -138 139 -18
59 -139 140 -19
60 -140 121 -20

//circle 2 end faces

81 41 -162 161
82 42 -163 162
83 43 -164 163
84 44 -165 164
85 45 -166 165
86 46 -167 166
87 47 -168 167
88 48 -169 168
89 49 -170 169
90 50 -171 170
91 51 -172 171
92 52 -173 172
93 53 -174 173
94 54 -175 174
95 55 -176 175
96 56 -177 176
97 57 -178 177
98 58 -179 178
99 59 -180 179
100 60 -161 180

//circle 3 end faces

1041 -1121 1122 -1001
1042 -1122 1123 -1002
1043 -1123 1124 -1003
1044 -1124 1125 -1004
1045 -1125 1126 -1005
1046 -1126 1127 -1006
1047 -1127 1128 -1007
1048 -1128 1129 -1008
1049 -1129 1130 -1009

1050 -1130 1131 -1010
1051 -1131 1132 -1011
1052 -1132 1133 -1012
1053 -1133 1134 -1013
1054 -1134 1136 -1014
1055 -1136 1135 5
1056 -1135 1137 -1016
1057 -1137 1138 -1017
1058 -1138 1139 -1018
1059 -1139 1140 -1019
1060 -1140 1121 -1020

//circle 4 end faces

1081 1041 -1162 1161
1082 1042 -1163 1162
1083 1043 -1164 1163
1084 1044 -1165 1164
1085 1045 -1166 1165
1086 1046 -1167 1166
1087 1047 -1168 1167
1088 1048 -1169 1168
1089 1049 -1170 1169
1090 1050 -1171 1170
1091 1051 -1172 1171
1092 1052 -1173 1172
1093 1053 -1174 1173
1094 1054 -1176 1174
1095 -45 -1175 1176
1096 1056 -1177 1175
1097 1057 -1178 1177
1098 1058 -1179 1178
1099 1059 -1180 1179
1100 1060 -1161 1180

bodies

1 1 2 3 4 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 1001 1002 1003 1004 1005 1006 1007 1008 1009 1010 1011 1012 1013 1014 1016 1017 1018 1019 1020 1041 1042 1043 1044 1045 1045 1046 1047 1048 1049 1050 1051 1052 1053 1054 1055 1056 1057 1058 1059 1060 1081 1082 1083 1084 1085 1086 1087 1088 1089 1090 1091 1092 1093 1094 1095 1096 1097 1098 1099 1100 volume 317.257447558279

Inequivalent Perpendicular NWs

//Radius of Small Cylinder

PARAMETER radiusS = 1

//Radius of Large Cylinder

PARAMETER radiusB= 3

//PARAMETER radtest=3

PARAMETER volumeamt=
(pi*radiusS*radiusS*2/3)+(pi*radiusB*radiusB*2/3)+(pi*radiusS*radiusS*50)+(pi*radiusB*radiusB*50)

//Sum of Both Radii, this is used for offset

PARAMETER radsum= radiusB +radiusS

vertices

//Cylinder 1 is small and is bisecting the xy plane

//Circles are centered at 0,1-cos(pi/20) in xy

//circle 1 vertices

1 radiusS*cos(0 + pi/20) 1-cos(pi/20)+radiusS*sin(0 + pi/20) -25
2 radiusS*cos(pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(pi/10 + pi/20) -25
3 radiusS*cos(2*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(2*pi/10 + pi/20) -25
4 radiusS*cos(3*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(3*pi/10 + pi/20) -25
5 radiusS*cos(4*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(4*pi/10 + pi/20) -25
6 radiusS*cos(5*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(5*pi/10 + pi/20) -25
7 radiusS*cos(6*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(6*pi/10 + pi/20) -25
8 radiusS*cos(7*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(7*pi/10 + pi/20) -25
9 radiusS*cos(8*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(8*pi/10 + pi/20) -25
10 radiusS*cos(9*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(9*pi/10 + pi/20) -25
11 radiusS*cos(10*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(10*pi/10 + pi/20) -25
12 radiusS*cos(11*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(11*pi/10 + pi/20) -25
13 radiusS*cos(12*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(12*pi/10 + pi/20) -25
14 radiusS*cos(13*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(13*pi/10 + pi/20) -25
15 radiusS*cos(14*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(14*pi/10 + pi/20) -25
16 radiusS*cos(15*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(15*pi/10 + pi/20) -25
17 radiusS*cos(16*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(16*pi/10 + pi/20) -25
18 radiusS*cos(17*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(17*pi/10 + pi/20) -25
19 radiusS*cos(18*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(18*pi/10 + pi/20) -25
20 radiusS*cos(19*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(19*pi/10 + pi/20) -25

//circle 2 vertices

41 radiusS*cos(0 + pi/20) 1-cos(pi/20)+radiusS*sin(0 + pi/20) 25
42 radiusS*cos(pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(pi/10 + pi/20) 25
43 radiusS*cos(2*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(2*pi/10 + pi/20) 25
44 radiusS*cos(3*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(3*pi/10 + pi/20) 25
45 radiusS*cos(4*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(4*pi/10 + pi/20) 25
46 radiusS*cos(5*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(5*pi/10 + pi/20) 25
47 radiusS*cos(6*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(6*pi/10 + pi/20) 25
48 radiusS*cos(7*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(7*pi/10 + pi/20) 25
49 radiusS*cos(8*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(8*pi/10 + pi/20) 25
50 radiusS*cos(9*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(9*pi/10 + pi/20) 25

51 radiusS*cos(10*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(10*pi/10 + pi/20) 25
52 radiusS*cos(11*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(11*pi/10 + pi/20) 25
53 radiusS*cos(12*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(12*pi/10 + pi/20) 25
54 radiusS*cos(13*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(13*pi/10 + pi/20) 25
55 radiusS*cos(14*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(14*pi/10 + pi/20) 25
56 radiusS*cos(15*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(15*pi/10 + pi/20) 25
57 radiusS*cos(16*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(16*pi/10 + pi/20) 25
58 radiusS*cos(17*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(17*pi/10 + pi/20) 25
59 radiusS*cos(18*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(18*pi/10 + pi/20) 25
60 radiusS*cos(19*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(19*pi/10 + pi/20) 25

//Cylinder 2 is is large and is bisecting the yz plane

//circle 3 vertices

1001 25 radiusB+cos(pi/20)+radiusB*cos(0 + pi/20) radiusB*sin(0 + pi/20)
1002 25 radiusB+cos(pi/20)+radiusB*cos(pi/10 + pi/20) radiusB*sin(pi/10 + pi/20)
1003 25 radiusB+cos(pi/20)+radiusB*cos(2*pi/10 + pi/20) radiusB*sin(2*pi/10 + pi/20)
1004 25 radiusB+cos(pi/20)+radiusB*cos(3*pi/10 + pi/20) radiusB*sin(3*pi/10 + pi/20)
1005 25 radiusB+cos(pi/20)+radiusB*cos(4*pi/10 + pi/20) radiusB*sin(4*pi/10 + pi/20)
1006 25 radiusB+cos(pi/20)+radiusB*cos(5*pi/10 + pi/20) radiusB*sin(5*pi/10 + pi/20)
1007 25 radiusB+cos(pi/20)+radiusB*cos(6*pi/10 + pi/20) radiusB*sin(6*pi/10 + pi/20)
1008 25 radiusB+cos(pi/20)+radiusB*cos(7*pi/10 + pi/20) radiusB*sin(7*pi/10 + pi/20)
1009 25 radiusB+cos(pi/20)+radiusB*cos(8*pi/10 + pi/20) radiusB*sin(8*pi/10 + pi/20)
1010 25 radiusB+cos(pi/20)+radiusB*cos(9*pi/10 + pi/20) radiusB*sin(9*pi/10 + pi/20)
1011 25 radiusB+cos(pi/20)+radiusB*cos(10*pi/10 + pi/20) radiusB*sin(10*pi/10 + pi/20)
1012 25 radiusB+cos(pi/20)+radiusB*cos(11*pi/10 + pi/20) radiusB*sin(11*pi/10 + pi/20)
1013 25 radiusB+cos(pi/20)+radiusB*cos(12*pi/10 + pi/20) radiusB*sin(12*pi/10 + pi/20)
1014 25 radiusB+cos(pi/20)+radiusB*cos(13*pi/10 + pi/20) radiusB*sin(13*pi/10 + pi/20)
1015 25 radiusB+cos(pi/20)+radiusB*cos(14*pi/10 + pi/20) radiusB*sin(14*pi/10 + pi/20)
1016 25 radiusB+cos(pi/20)+radiusB*cos(15*pi/10 + pi/20) radiusB*sin(15*pi/10 + pi/20)
1017 25 radiusB+cos(pi/20)+radiusB*cos(16*pi/10 + pi/20) radiusB*sin(16*pi/10 + pi/20)
1018 25 radiusB+cos(pi/20)+radiusB*cos(17*pi/10 + pi/20) radiusB*sin(17*pi/10 + pi/20)
1019 25 radiusB+cos(pi/20)+radiusB*cos(18*pi/10 + pi/20) radiusB*sin(18*pi/10 + pi/20)
1020 25 radiusB+cos(pi/20)+radiusB*cos(19*pi/10 + pi/20) radiusB*sin(19*pi/10 + pi/20)

//circle 4 vertices

1041 -25 radiusB+cos(pi/20)+radiusB*cos(0 + pi/20) radiusB*sin(0 + pi/20)
1042 -25 radiusB+cos(pi/20)+radiusB*cos(pi/10 + pi/20) radiusB*sin(pi/10 + pi/20)
1043 -25 radiusB+cos(pi/20)+radiusB*cos(2*pi/10 + pi/20) radiusB*sin(2*pi/10 + pi/20)
1044 -25 radiusB+cos(pi/20)+radiusB*cos(3*pi/10 + pi/20) radiusB*sin(3*pi/10 + pi/20)
1045 -25 radiusB+cos(pi/20)+radiusB*cos(4*pi/10 + pi/20) radiusB*sin(4*pi/10 + pi/20)
1046 -25 radiusB+cos(pi/20)+radiusB*cos(5*pi/10 + pi/20) radiusB*sin(5*pi/10 + pi/20)
1047 -25 radiusB+cos(pi/20)+radiusB*cos(6*pi/10 + pi/20) radiusB*sin(6*pi/10 + pi/20)
1048 -25 radiusB+cos(pi/20)+radiusB*cos(7*pi/10 + pi/20) radiusB*sin(7*pi/10 + pi/20)
1049 -25 radiusB+cos(pi/20)+radiusB*cos(8*pi/10 + pi/20) radiusB*sin(8*pi/10 + pi/20)
1050 -25 radiusB+cos(pi/20)+radiusB*cos(9*pi/10 + pi/20) radiusB*sin(9*pi/10 + pi/20)
1051 -25 radiusB+cos(pi/20)+radiusB*cos(10*pi/10 + pi/20) radiusB*sin(10*pi/10 + pi/20)
1052 -25 radiusB+cos(pi/20)+radiusB*cos(11*pi/10 + pi/20) radiusB*sin(11*pi/10 + pi/20)
1053 -25 radiusB+cos(pi/20)+radiusB*cos(12*pi/10 + pi/20) radiusB*sin(12*pi/10 + pi/20)
1054 -25 radiusB+cos(pi/20)+radiusB*cos(13*pi/10 + pi/20) radiusB*sin(13*pi/10 + pi/20)
1055 -25 radiusB+cos(pi/20)+radiusB*cos(14*pi/10 + pi/20) radiusB*sin(14*pi/10 + pi/20)
1056 -25 radiusB+cos(pi/20)+radiusB*cos(15*pi/10 + pi/20) radiusB*sin(15*pi/10 + pi/20)
1057 -25 radiusB+cos(pi/20)+radiusB*cos(16*pi/10 + pi/20) radiusB*sin(16*pi/10 + pi/20)

1058 -25 radiusB+cos(pi/20)+radiusB*cos(17*pi/10 + pi/20) radiusB*sin(17*pi/10 + pi/20)
1059 -25 radiusB+cos(pi/20)+radiusB*cos(18*pi/10 + pi/20) radiusB*sin(18*pi/10 + pi/20)
1060 -25 radiusB+cos(pi/20)+radiusB*cos(19*pi/10 + pi/20) radiusB*sin(19*pi/10 + pi/20)

//end centers Cylinder 1 Small

81 0 0 -27
82 0 0 27

//end centers Cylinder 2 Big

//Shift cylinder 2 in y by rB+rS

1081 27 radsum 0
1082 -27 radsum 0

//connection points both cylinders

83 radiusS*cos(4*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(4*pi/10 + pi/20) 0-radiusB*sin(pi/20)
84 radiusS*cos(5*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(5*pi/10 + pi/20) 0-radiusB*sin(pi/20)
85 radiusS*cos(4*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(4*pi/10 + pi/20) 0+radiusB*sin(pi/20)
86 radiusS*cos(5*pi/10 + pi/20) 1-cos(pi/20)+radiusS*sin(5*pi/10 + pi/20) 0+radiusB*sin(pi/20)

edges

//circle 1 edges

1 1 2
2 2 3
3 3 4
4 4 5
5 5 6
6 6 7
7 7 8
8 8 9
9 9 10
10 10 11
11 11 12
12 12 13
13 13 14
14 14 15
15 15 16
16 16 17
17 17 18
18 18 19
19 19 20
20 20 1

//circle 2 edges

41 41 42
42 42 43
43 43 44

44 44 45
45 45 46
46 46 47
47 47 48
48 48 49
49 49 50
50 50 51
51 51 52
52 52 53
53 53 54
54 54 55
55 55 56
56 56 57
57 57 58
58 58 59
59 59 60
60 60 41

//circle 3 edges

1001 1001 1002
1002 1002 1003
1003 1003 1004
1004 1004 1005
1005 1005 1006
1006 1006 1007
1007 1007 1008
1008 1008 1009
1009 1009 1010
1010 1010 1011
1011 1011 1012
1012 1012 1013
1013 1013 1014
1014 1014 1015
1015 1015 1016
1016 1016 1017
1017 1017 1018
1018 1018 1019
1019 1019 1020
1020 1020 1001

//circle 4 edges

1041 1041 1042
1042 1042 1043
1043 1043 1044
1044 1044 1045
1045 1045 1046
1046 1046 1047
1047 1047 1048
1048 1048 1049
1049 1049 1050
1050 1050 1051
1051 1051 1052

1052 1052 1053
1053 1053 1054
1054 1054 1055
1055 1055 1056
1056 1056 1057
1057 1057 1058
1058 1058 1059
1059 1059 1060
1060 1060 1041

//connect circle 1 to circle 2

81 1 41
82 2 42
83 3 43
84 4 44
//85 5 45
//86 6 46
87 7 47
88 8 48
89 9 49
90 10 50
91 11 51
92 12 52
93 13 53
94 14 54
95 15 55
96 16 56
97 17 57
98 18 58
99 19 59
100 20 60

//connect circle 3 to circle 4

1081 1001 1041
1082 1002 1042
1083 1003 1043
1084 1004 1044
1085 1005 1045
1086 1006 1046
1087 1007 1047
1088 1008 1048
1089 1009 1049
//1090 1010 1050
//1091 1011 1051
1092 1012 1052
1093 1013 1053
1094 1014 1054
1095 1015 1055
1096 1016 1056
1097 1017 1057
1098 1018 1058
1099 1019 1059
1100 1020 1060

//Circle 1 connect to center

121 81 1
122 81 2
123 81 3
124 81 4
125 81 5
126 81 6
127 81 7
128 81 8
129 81 9
130 81 10
131 81 11
132 81 12
133 81 13
134 81 14
135 81 15
136 81 16
137 81 17
138 81 18
139 81 19
140 81 20

//Circle 2 connect to center

161 82 41
162 82 42
163 82 43
164 82 44
165 82 45
166 82 46
167 82 47
168 82 48
169 82 49
170 82 50
171 82 51
172 82 52
173 82 53
174 82 54
175 82 55
176 82 56
177 82 57
178 82 58
179 82 59
180 82 60

//Circle 3 connect to center

1121 1081 1001
1122 1081 1002
1123 1081 1003

1124 1081 1004
1125 1081 1005
1126 1081 1006
1127 1081 1007
1128 1081 1008
1129 1081 1009
1130 1081 1010
1131 1081 1011
1132 1081 1012
1133 1081 1013
1134 1081 1014
1135 1081 1015
1136 1081 1016
1137 1081 1017
1138 1081 1018
1139 1081 1019
1140 1081 1020

//Circle 4 connect to center

1161 1082 1041
1162 1082 1042
1163 1082 1043
1164 1082 1044
1165 1082 1045
1166 1082 1046
1167 1082 1047
1168 1082 1048
1169 1082 1049
1170 1082 1050
1171 1082 1051
1172 1082 1052
1173 1082 1053
1174 1082 1054
1175 1082 1055
1176 1082 1056
1177 1082 1057
1178 1082 1058
1179 1082 1059
1180 1082 1060

//Connect circle 1 to center
200 5 83
201 6 84

//Connect circle 2 to center
202 45 85
203 46 86

//Connect circle 3 to center
204 1010 85
205 1011 83

//Connect circle 4 to center
206 1050 86

207 1051 84

//Center square
208 83 85
209 85 86
210 86 84
211 84 83

faces

//Cyl 1 side faces, negative sign traverses vector in direction opposite to definition

1 1 82 -41 -81
2 2 83 -42 -82
3 3 84 -43 -83
//4 4 85 -44 -84
//5 5 86 -45 -85
//6 6 87 -46 -86
7 7 88 -47 -87
8 8 89 -48 -88
9 9 90 -49 -89
10 10 91 -50 -90
11 11 92 -51 -91
12 12 93 -52 -92
13 13 94 -53 -93
14 14 95 -54 -94
15 15 96 -55 -95
16 16 97 -56 -96
17 17 98 -57 -97
18 18 99 -58 -98
19 19 100 -59 -99
20 20 81 -60 -100

//Faces involving midpoints

21 5 201 211 -200
22 202 209 -203 -45
23 204 -208 -205 -1010//1010 205 208 -204
24 1050 207 -210 -206
25 6 87 -46 203 210 -201
26 4 200 208 -202 -44 -84
27 205 -211 -207 1051 -1092 -1011//1011 1092 -1051 207 211 -205
28 1089 1049 206 -209 -204 -1009//1009 204 209 -206 -1049 -1089
//29 208 209 210 211

//Cyl2 side faces

1001 1081 1041 -1082 -1001
1002 1082 1042 -1083 -1002
1003 1083 1043 -1084 -1003
1004 1084 1044 -1085 -1004
1005 1085 1045 -1086 -1005
1006 1086 1046 -1087 -1006
1007 1087 1047 -1088 -1007
1008 1088 1048 -1089 -1008

//1009 1009 1090 -1049 -1089
//1010 1010 1091 -1050 -1090
//1011 1011 1092 -1051 -1091
1012 1092 1052 -1093 -1012
1013 1093 1053 -1094 -1013
1014 1094 1054 -1095 -1014
1015 1095 1055 -1096 -1015
1016 1096 1056 -1097 -1016
1017 1097 1057 -1098 -1017
1018 1098 1058 -1099 -1018
1019 1099 1059 -1100 -1019
1020 1100 1060 -1081 -1020

//circle 1 end faces

41 -121 122 -1
42 -122 123 -2
43 -123 124 -3
44 -124 125 -4
45 -125 126 -5
46 -126 127 -6
47 -127 128 -7
48 -128 129 -8
49 -129 130 -9
50 -130 131 -10
51 -131 132 -11
52 -132 133 -12
53 -133 134 -13
54 -134 135 -14
55 -135 136 -15
56 -136 137 -16
57 -137 138 -17
58 -138 139 -18
59 -139 140 -19
60 -140 121 -20

//circle 2 end faces

81 41 -162 161
82 42 -163 162
83 43 -164 163
84 44 -165 164
85 45 -166 165
86 46 -167 166
87 47 -168 167
88 48 -169 168
89 49 -170 169
90 50 -171 170
91 51 -172 171
92 52 -173 172
93 53 -174 173
94 54 -175 174
95 55 -176 175
96 56 -177 176
97 57 -178 177

98 58 -179 178
99 59 -180 179
100 60 -161 180

//circle 3 end faces

1041 1001 -1122 1121
1042 1002 -1123 1122
1043 1003 -1124 1123
1044 1004 -1125 1124
1045 1005 -1126 1125
1046 1006 -1127 1126
1047 1007 -1128 1127
1048 1008 -1129 1128
1049 1009 -1130 1129
1050 1010 -1131 1130
1051 1011 -1132 1131
1052 1012 -1133 1132
1053 1013 -1134 1133
1054 1014 -1135 1134
1055 1015 -1136 1135
1056 1016 -1137 1136
1057 1017 -1138 1137
1058 1018 -1139 1138
1059 1019 -1140 1139
1060 1020 -1121 1140

//circle 4 end faces

1081 -1161 1162 -1041
1082 -1162 1163 -1042
1083 -1163 1164 -1043
1084 -1164 1165 -1044
1085 -1165 1166 -1045
1086 -1166 1167 -1046
1087 -1167 1168 -1047
1088 -1168 1169 -1048
1089 -1169 1170 -1049
1090 -1170 1171 -1050
1091 -1171 1172 -1051
1092 -1172 1173 -1052
1093 -1173 1174 -1053
1094 -1174 1175 -1054
1095 -1175 1176 -1055
1096 -1176 1177 -1056
1097 -1177 1178 -1057
1098 -1178 1179 -1058
1099 -1179 1180 -1059
1100 -1180 1161 -1060

bodies
1 1 2 3 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 25 26 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 23 24 27 28 1001 1002 1003 1004 1005 1006 1007 1008 1012 1013 1014 1015 1016 1017 1018 1019 1020 1041 1042 1043 1044 1045 1045 1046 1047 1048

1049 1050 1051 1052 1053 1054 1055 1056 1057 1058 1059 1060 1081 1082 1083 1084 1085 1086 1087 1088
1089 1090 1091 1092 1093 1094 1095 1096 1097 1098 1099 1100 volume volumeamt

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